JEPPIAAR ENGINEERING COLLEGE

Jeppiaar Nagar, Rajiv Gandhi Salai, Chennai – 119

DEPARTMENT OF INFORMATION TECHNOLOGY

2009-2010 Even Semester
SEMESTER IV

Unit wise 2 mark and 16 mark Questions with Answers
(As per Anna University syllabus)

MA2262 PROBABILITY AND QUEUEING THEORY

(Common to CSE & IT)

SYLLABUS

UNIT I RANDOM VARIABLES 9+3

Discrete and continuous random variables - Moments - Moment generating functions and their properties. Binomial, Poisson ,Geometric ,Negative binomial, Uniform, Exponential, Gamma, and Weibull distributions .

UNIT II TWO DIMENSIONAL RANDOM VARIABLES 9+3

Joint distributions - Marginal and conditional distributions – Covariance - Correlation and regression - Transformation of random variables - Central limit theorem.

UNIT III MARKOV PROCESSES AND MARKOV CHAINS 9+3

Classification - Stationary process - Markov process - Markov chains - Transition probabilities - Limiting distributions-Poisson process

UNIT IV QUEUEING THEORY 9+3

Markovian models – Birth and Death Queuing models- Steady state results: Single and multiple server queuing models- queues with finite waiting rooms- Finite source models- Little's Formula

UNIT V NON-MARKOVIAN QUEUES AND QUEUE NETWORKS 9+3

M/G/1 queue- Pollaczek- Khintchine formula, series queues- open and closed networks

TUTORIAL 15
TOTAL : 60

TEXT BOOKS

1. O.C. Ibe, "Fundamentals of Applied Probability and Random Processes", Elsevier, 1st Indian Reprint, 2007 (For units 1, 2 and 3).
2. D. Gross and C.M. Harris, "Fundamentals of Queueing Theory", Wiley Student edition, 2004 (For units 4 and 5).

BOOKS FOR REFERENCES

1. A.O. Allen, "Probability, Statistics and Queueing Theory with Computer Applications", Elsevier, 2nd edition, 2005.
1. H.A. Taha, "Operations Research", Pearson Education, Asia, 8th edition, 2007.
3. K.S. Trivedi, "Probability and Statistics with Reliability, Queueing and Computer Science Applications", John Wiley and Sons, 2nd edition, 2002.

UNIT I

RANDOM VARIABLES

PART – A

1. If Var(x) = 4, find Var (3x+8), where X is a random variable.
   Solution: Var (ax+b) = a^2 Var x
   Var (3x+8) = 3^2 Var x = 36

2. If a random variable X takes the values 1,2,3,4 such that 2P(X=1) = 3P(X=2) = P(X=3) = 5P(x=4). Find the probability distribution of X.
   Solution: Let P(X=3)= k,
   P(X=1) = k/2
   P(X=2) = k/3
   P(X=4) = k/5

$$\frac{k}{2}+\frac{k}{3}+k+\frac{k}{5}=1$$

$$\Rightarrow\ k=\frac{30}{61}$$

   P(X=1) = 15/61
   P(X=2) = 10/61
   P(X=3)= 30/61
   P(X=4)= 6/61

3. A continuous random variable X has probability density function given by f(x) = $3x^2$ 0,x,1. Find K such that P(X>K) = 0.05.
   Solution:

$$P(X \le K) = 0.95$$

$$\int_0^K 3x^2 dx = 0.5 \qquad \Rightarrow K^3 = 0.95$$

$$K = (0.95)^{\frac{1}{3}} = 0.983$$

4. Find the cumulative distribution fuction F(x) corresponding to the p.d.f. f(x) = $\frac{1}{\pi(1+x^2)}$,$-\infty < x < \infty$

Solution:

$$F(x) = \int_{-\infty}^{x} \frac{1}{\pi(1+x^2)}\,dx$$

$$= \frac{1}{\pi}\left[\tan^{-1} x\right]_{-\infty}^{x}$$

$$= \frac{1}{\pi}\tan^{-1} x + \frac{1}{2}$$

5. If a RV X has the moment generating function $M_x(t) = \frac{2}{2-t}$

   Determine the variance of X.

   Solution:

$$M_x(t) = \frac{2}{2-t} = \left(1 - \frac{t}{2}\right)^{-1}$$

$$E(X) = \frac{1}{2} \quad E(X^2) = \frac{1}{2}$$

$$Var(x) = E(X^2) - \left(E(X)\right)^2 = \frac{1}{4}$$

6. In a binomial distribution the mean is 4 and variance is 3, Find P(X=0).

   Solution: np=4, npq=3

   Hence q=3/4, p=1-q=1/4,

   Since np=4 , n=16.

$$P(X = x) = nc_x p^x q^{n-x}$$

$$= 16c_x \left(\frac{1}{4}\right)^x \left(\frac{3}{4}\right)^{16-x} \quad x = 0,1,2,...$$

$$P9X = 0) = \left(\frac{3}{4}\right)^{16} = 0.01002$$

7. The moment generating function of a random variable X is given by $M_x(t) = e^{3(e^t-1)}$. Find P(X=1).

   Solution: λ= 3

$$f(x) = \frac{e^{-3}3^x}{x!},\ x = 1,2,3,...$$

$$P(X = 1) = \frac{e^{-3}3^1}{1!} = 0.1494$$

8. Find the moment generating function of uniform distribution.

$$M_x(t) = \int_{-\infty}^{\infty} e^{tx} f(x)dx$$

Solution: $$= \int_a^b e^{tx} \frac{1}{b-a} dx$$

$$= \frac{e^{bt} - e^{at}}{t(b-a)}$$

9. What are the properties of Normal distribution?
   Solution:
   - The normal curve is symmetrical when p=q or $p \approx q$
   - The normal curve is a single peaked curve
   - The normal curve is asymptotic to x-axis as y decreases rapidly when x increases numerically.
   - The mean, median and mode coincide and lower and upper quartiles are equidistant from the median
   - The curve is completely specified by mean and standard deviation along with the value of y_o

10. The life time of a component measured in hours is Weibull distribution with parameter $\alpha = 0.2,\ \beta = 0.5.$ Find the mean lifeti;me of the component.
    Solution:

    Mean = E(X)= $\alpha^{-1/\beta}\Gamma\left(1+\frac{1}{\beta}\right)$

    The mean life of the component = $0.2^{-1/0.5}\Gamma\left(1+\frac{1}{0.5}\right) = 50\ hours$

11. If X is binomially distributed with n=6 such that P(X=2)=9P(X=4), find E(x) and Var(x).
    Solution: $6C_2\ p^2q^4 = 9\ (6C_4\ p^4q^2)$; q=3p ;p=1/4.
    E(X)=1.5 ; Var(X) = 9/8

13. If $f(x) = kx^2$, 0<x<3, is to be a density function, find the value of k.

    Solution: $\int_0^3 kx^2 dx = 1; 9k = 1; k = \frac{1}{9}$

PART – B

Refer: (A) Probability and statistics by M. Sundravalli and R. Mahadevan
(B) Probability and statistics by T. Veerarajan.
(C) Probability Queueing Theory by G. Balaji.

1. Find the mean and variance of the following distributions: Binomial, Poisson(Refer B: page no:179,183)

2. Find the mean and variance of the following distributions : Geometric and Exponential(Refer B : page no:185,212)

3. Prove that Poisson distribution is the limiting form of Binomial distribution.
(Refer B: page no : 181)

4. For a triangular distribution $f(x) = \begin{cases} x, & 0 < x \le 1 \\ 2 - x & 1 \le x \le 2 \\ 0 & otherwise \end{cases}$
Find the mean, variance and moment generating function.
(Refer C: page no : 1.122)

5.It is known that the probability of an item produced by a certain machine will be defective is 0.05. If the produced items are sent to the market in packets of 20, fine the no. of packets containing at least, exactly and atmost 2 defective items in a consignment of 1000 packets using (i) Binomial distribution (ii) Poisson approximation to binomial distribution.
(Refer C: page no : 2.28)

6. The daily consumption of milk in excess of 20,000 gallons is approximately exponentially distributed with $\theta = 3000$. The city has a daily stock of 35,000 gallons. What is the probability that of two days selected at random, the stock is insufficient for both days.
(Refer C: page no : 2.74)

7. Each of the 6 tubes of a radio set has a life length (in yrs) which may be considered as a RV that follows a weibull distribution with parameters $\alpha = 25 \; and \; \beta = 2$. If these tubes function independently of one another,

what is the probability that no tube will have to be replaced during the first 2 months of service?
(Refer C: page no : 2.82)

UNIT II

TWO- DIMENSIONAL RANDOM VARIABLES

PART – A

1. State Central limit theorem.
   Solution: If X is the mean of a sample of size n taken from a population having the mean μ and the finite variance σ^2, then

$Z = \dfrac{X-\mu}{\sigma/\sqrt{n}}$ is a random variable whose distribution function approaches that of the standard normal distributions as n tends to infinity.

2. Define discrete probability Distribution.

   Solution: The mathematical definition of a discrete probability function, p(x) is a function that satisfies the following properties.

   a) The probability that x can take a specific value is p(x). That is $P(X=x)=p(x)=p_x$
   b) P(x) is non-negative for all real x.
   c) The sum of p(x) over all possible values of x is 1, that is $\sum p(j) = 1$ where j represents all possible values that x can have and p_j is the probability at x_j.

3. What is conditional probability?

   Solution: The conditional probability of X given Y is $f(y/x)= f(x,y)/f_2(y)$.

4. Define Marginal distribution function.

   Solution: $P(X \le x) = F_1(x) = \int_{u=-\infty}^{x} \int_{v=-\infty}^{\infty} f(u,v)dudv$

   $P(Y \le y) = F_2(x) = \int_{u=-\infty}^{\infty} \int_{v=-\infty}^{y} f(u,v)dudv$

   The above eqns are called the marginal distribution functions or distribution functions of X and Y.

5. Define Marginal density function.

   Solution: $P(X \le x) = F_1(x) = \int_{u=-\infty}^{x} \int_{v=-\infty}^{\infty} f(u,v)dudv$

   $P(Y \le y) = F_2(x) = \int_{u=-\infty}^{\infty} \int_{v=-\infty}^{y} f(u,v)dudv$

   The derivatives of the above equations with respect to x and y are then called the marginal density functions or simply the density functions, of X and Y and are given by $f_1(x)= \int_{v=-\infty}^{\infty} f(x,y)dv$ $f_2(y)= \int_{u=-\infty}^{\infty} f(x,y)du$

6. What is Covariance?

Solution: If X and Y are two random variables with the respective expected values $\overline{X}$, $\overline{Y}$ then the covariance between X and Y is defined by the relation μ_{11}=Cov(X,Y)=E((X-$\overline{X}$)(Y-$\overline{Y}$))

7. Define regression.
Solution: The main purpose of curve fitting is to estimate one of the variables (the dependent variable) from the other(the independent variable). The process of estimation is often referred to as regression.

8. What is a scatter diagram?
Solution: A scatter diagram is a graphical representation of data points for a particular sample. Choosing a different sample, or enlarging the original one can obtain a different scatter diagram.

9. If X represents the total number of heads obtained, when a fair coin is tossed 5 times, find the probability distribution of X.
Soln.:

X	0	1	2	3	4	5
P_x	1/32	5/32	10/32	10/32	5/32	1/32

10. If the probability distribution of X is given as:

x	1	2	3	4
P_x	0.4	0.3	0.2	0.1

Find $P\left(\frac{1}{2} < X < \frac{7}{2} / X > 1\right)$.

Solution: $\frac{P\left\{\left(\frac{1}{2} < X < \frac{7}{2}\right) \cap (X > 1)\right\}}{P(X > 1)} = \frac{P(X = 2 or 3)}{P(X = 2,3 or 4)} = \frac{0.5}{0.6} = \frac{5}{6}$

11. If the pdf of X is f(x)=2x , 0<x<1, find the pdf of (i)Y=3X+1.
(ii) y=$\sqrt{X}$

Solution: (i) f(y) = $\left|\frac{dx}{dy}\right| f(x) = \frac{2}{9}(y-1) in 1 < y < 4$

(ii)f(y) = 2y x $2y^2 = 4y^3$ in 0 <y <1.

12. If the RV X is uniformly distributed in (0,2), find the pdf of

$Y= X^3$.

Solution: $f(y) = \left|\frac{1}{2} y^{-\frac{2}{3}}\right| \frac{1}{2} = \frac{1}{6} y^{-\frac{2}{3}}$ $0 <y<8$.

13. If the R.V X is uniformly distributed in (-1,1) , find the pdf of $Y = |X|$.

Solution: $f(y) = \frac{1}{2} + \frac{1}{2} = 1$ in $0 < y < 1$.

14. If the joint pdf of (X,Y) is given by $f(x,y)=2$ in $0 \le x < y \le 1$. Find E(x).

Solution: $E(x) = \int_0^1 \int_0^y 2x\,dx\,dy = \int_0^1 y^2\,dy = \frac{1}{3}$

15. When are 2 random variables orthogonal?

Solution: If $E(XY)= 0$.

PART – B

Refer: (A) Probability and statistics by M. Sundravalli and R. Mahadevan
(B) Probability and statistics by T. Veerarajan.
(C) Probability Queueing Theory by G. Balaji.

1. State and prove the central limit theorem for independent and identically distributed random variables.
Solution: Refer(B) page no: 165.

2. (a) If X_1 and X_2 are independent Poisson variates with parameters λ_1 and λ_2, find the conditional distribution of X_1 for a given X_1+X_2.

(b).The joint density function of 2 continuous random variables X and Y is $f(x,y) = \begin{cases} c\,xy, & 0<x<4,\ 1<y<5 \\ 0 & \text{otherwise} \end{cases}$

1.Find $P[X \ge 3, Y \le 2]$

2.Find marginal distribution function of X.

Solution: Refer (A) page no: 81-86

3. The joint density function of a RV (X,Y) is
   f(x,y)= 8xy , 0 <x<1; 0<y<x;
   Find the marginal density functions.
   Find the conditional density function f(y/x).
   Solution: Refer (B) page no: 81(prob 34).

4. The joint pdf of the RV (X,Y) is given by
   $f(x,y) = kxy\,e^{-(x^2+y^2)}$, x>0 , y>0
   Find the value of k and prove also that X and Y are independent.
   Solution: Refer (B) page no: 73.

5. The joint probability mass function of (X,Y) is given by p(x,y) = k(2x + 3y); x=0,1,2; y=1,2,3.
   Find all the marginal and conditional probability distributions. Also find the probability distribution of (X+Y).
   Solution: Refer (B) page no:65.

6. If X and Y are independent RVs each following N(0,2),
   Find the pdf of Z=2X+3Y.
   Solution: Refer (B) : page no :106.

7. If X and Y each follow an exponential distribution with parameter 1 and are independent , find the pdf of U=X-Y.
   Solution: Refer (B) : page no : 107.

8. If the joint pdf of (X,Y) is given by f(x,y) = x+y ; $0 \le x,y \le 1$, find the pdf of U=XY.
   Solution: Refer (B) : page no : 108.
9. If X and Y are independent RVs with $f(x) = e^{-x}\,U(x)$ and $f(y)= 3e^{-3y}\,U(y)$, find f(z) if Z=X/Y
   Solution: Refer (B): page no:109.

10. If X,Y and Z are uncorrelated RVs with zero means and standard deviations 5,12 and 9 respectively and if U=X+Y and V=Y+Z, find the correlation coefficient between U and V.
    Solution: Refer B : page no: 132

11. If the joint pdf of (X,Y) is given by $f(x,y) = x + y$, $0 \le x, y \le 1$, find ρ_{xy}.
Solution: Refer B: page no:140 (prob 64).

12. The lifetime of a certain brand of an electric bulb may be considered a RV with mean 1200 h and standard deviation 250h. Find the probability, using central limit theorem, that the average lifetime of 60 bulbs exceeds 1250 h.
Solution: Refer B: page no : 165

13. A distribution with unknown mean has variance equal to 1.5. Use Central limit theorem to find how large a sample should be taken from the distribution in order that the probability will be atleast 0.95 that the sample mean will be within 0.5 of the population mean.
Solution: Refer B: page no :166

14. If $X_1, X_2, \ldots, X_n$ are Poisson variates with parameter $\lambda=2$, use central limit theorem to estimate $P(120 \le S_n \le 160)$, where $S_n = X1+X2+\ldots+X_n$ and $n=75$.
Solution: Refer B: page no: 167.

15. The joint pdf of a two dimensional RV (X,Y) is given by $f(x,y)= xy^2 + x^2/8$, $0 \le x \le 2$, $0 \le y \le 1$. Compute $P(X \ge 1)$, $P(Y< ½)$, $P(x >1/y < 1/2)$, $P(X < Y)$
Solution: REFER (B) , pg no : 69

UNIT III

MARKOV PROCESSES AND MARKOV CHAINS

REFERENCE : "PROBABILITY, STATISTICS & RANDOM PROCESS " - T. VEERARAJAN

PART A

1. Define Random process. (Pg – 337)
Solution: A random process is a collection of random variables {X(s,t)} that are functions of a real variable, namely t where

$s \in$ (sample space) and $t \in T$(parameter set).

2. Give the classification of Random Processes.(Pg – 338)
   Solution: Discrete random sequence, Continuous random sequence, Discrete random process, Continuous random process.

3. Define Stationary processes. (Pg – 339)
   Solution: If certain probability distribution or averages do not depend on t, then the random process {X(t)} is called stationary.

4. Define SSS process.(Pg – 340)
   Solution: A random process is called a strongly stationary process or strict sense stationary process, if all its finite dimensional distributions are invariant under translation of time parameter.

5. Define WSS process.(Pg – 341)
   Solution: A random process {X(t)} with finite first and second order moments is called a weakly stationary process or covariance stationary process or wide-sense stationary process, if its mean is a constant and the auto correlation depends only on the time difference.

6. Is Poisson process covariance stationary? Justify.(Pg – 343)
   Solution: No. Mean of poisson process = $\lambda t \neq$ a constant.

7. Show that the random process $X(t)=A\cos(w_0 t + \theta)$ is WSS, if A and w_0 are constants and θ is a uniformly distributed RV in $(0 , 2\pi)$. (Pg – 344)
   Solution: Mean = 0 = a constant.
   Autocorrelation = $(A^2/2)\cos w_0 (t_1 - t_2)$.
   Hence WSS process.

8. If {X(t)} is a wss process with autocorrelation $R(\tau)=Ae^{-\alpha|\tau|}$, determine the second-order moment of the RV X(8) – X(5).
   Solution: $2A(1 - e^{-3\alpha})$

9. Define Markov process. (Pg – 446)
   Solution: Markov process is one in which the future value is independent of the past values, given the present value

10. Define Markov chain.(Pg – 447).

Solution: Random processes with Markov property which takes discrete values, whether t is discrete or continuous, are called Markov chains.

11. Prove that the matrix $\begin{pmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1/2 & 1/2 & 0 \end{pmatrix}$ is the tpm of the irreducible Markov chain. (Pg – 458 ;eg: 7)

12. . State Chapman-Kolmogorov theorem.(Pg – 448)

Solution: If P is the tpm of a homogeneous Markov chain, then the n-step tpm $P^{(n)} = P^n$.

13. If the tpm of a Markov chain is $\begin{pmatrix} 0 & 1 \\ 1/2 & 1/2 \end{pmatrix}$ find the steady-state distribution of the chain.(Pg – 460)

Sol: 1/3 , 2/3

PART B

1(a). Define Poisson Process.(Pg – 434)

Derive the Probability Law for the Poisson Process. (Pg – 435).

(b). What is the mean and autocorrelation of the Poisson Process?(Pg – 436)

2(a). Prove that the interarrival time of a Poisson process with parameter λ has an exponential distribution with mean $(1 / \lambda)$. (Pg – 438)

(b). If the customers arrive at a bank according to a Poisson process with mean rate of 2 per minute, find the

probability that, during a 1 – min interval, no customer arrives.(Pg 444)

3. A radioactive source emits particles at rate of 5 per minute in accordance with Poisson process. Each particle emitted has a probability 0.6 of being recorded. Find the probability that 10 particles are recorded in 4 – min period. (Pg – 442)

4. Patients arrive randomly and independently at a doctor's consulting room from 8 A.M. at an average rate of one in 5 min. The waiting room can hold 12 persons. What is the probability that the room will be full when the doctor arrives at 9 A.M.?(Pg – 445)

5. Suppose that the customers arrive at a counter independently from 2 different sources. Arrivals occur in accordance with a Poisson process with mean rate of 6 per hour from the first source and 4 per hour from the second source. Find the mean interval between any 2 successives arrivals.(Pg – 445)

6. Define Autocorrelation and Autocovariance of the Random process.(Pg – 340)
Define Correlation coefficient, Cross-correlation,cross-covariance of Random process. (Pg – 340).
Define Random walk.(Pg-350)
Define a semirandom telegraph signal process and random telegraph signal process . Are they stationary? (Pg -353)

7. State and prove the additive property of Poisson process. (Pg – 437)
Prove that the difference of 2 independent Poisson Process is not a Poisson Process. (Pg – 438)

8. A man either drives a car or catches a train to go to office each day. He never goes 2 days in a row by train but if he drives one day, then the next day he is just as likely to drive again as he is to travel by train. Now suppose that on the first day of the week, the man tossed a fair dice and drove to work if and only if a 6 appeared. Find (a) the probability that he takes a train on the third day and (b) the probability he drives to work in the long run.(Pg –453 ; eg:3)

9. A gambler has Rs. 2/- . He bets Rs.1 at a time and wins Rs.1 with probability ½. He stops playing if he loses Rs.2 or wins Rs.4. (a)what is the tpm of the related Markov chain? (b) What is the probability that he has lost his money at the end of 5 plays? (c) What is the probability that the same game lasts more than 7 plays?(Pg-456)

10. There are 2 white marbles in urn A and 3 red marbles in urn B. At each step of the process, a marble is selected from each urn and the 2 marbles selected are interchanged. Let the state a_I of the system be the number of red marbles in A after i changes. What is the probability that there are 2 red marbles in urn A?(Pg –457)

11. Three boys A,B and C are throwing a ball to each other. A always throws the ball to B and B always throws the ball to C, but C is just as likely to throw the ball to B as to A. Show that the process is Markovian. Find the transition matrix and classify the states. (Pg – 459).

UNIT IV

QUEUEING THEORY

PART A

1. What are the characteristics of a queueing system?
   Solution: (i) The input pattern
   (ii) The service mechanism
   (iii)The queue discipline

2. What do you mean by transient state and steady-state queueing systems?

Solution: If the characteristics of a queueing system are independent of time or equivalently if the behaviour of the system is independent of time, the system is said to be in steady-state. Otherwise it is said to be in transient-state.

3. Write down the Little's formula that hold good for the infinite capacity Poisson queue models.

   Solution: (i) $E(N_s) = \frac{\lambda}{\mu - \lambda} = \lambda E(W_s)$

   (ii) $E(N_q) = \frac{\lambda^2}{\mu(\mu - \lambda)} = \lambda E(W_q)$

   (iii) $E(W_s) = E(W_q) + \frac{1}{\mu}$

   (iv) $E(N_s) = E(N_q) + \frac{\lambda}{\mu}$

4. If a customer has to wait in a (M/M/1):(∞/FIFO) queue system, What is his average waiting time in the queue, if λ=8 per hour and μ=12 per hour.
   Solution: 5 min.

5. If there are 2 servers in an infinite capacity Poisson queue system with λ=10 per hour and μ=15 per hour,what is the percentage of idle time for each server.
   Solution: 50%

6. In a 3 server infinite capacity Poisson queue model if λ/sμ=2/3 Find P_0.
   Solution : 1/9
7. If λ/sμ=2/3 in a (M/M/s):(∞/FIFO) queue system find the average number of customers in the nonempty queue.
   Solution: 2

8. What is the probability that an arrival to infinite capacity 3 server infinite capacity Poisson queue with λ/sμ=2/3 and P_0=1/9 enters the service without waiting?
   Solution : 5/9

9. What is the average waiting time of a customer in the 3 server infinite capacity Poisson queue if he happens to wait, given that λ=6 per hour and μ=4 per hour.
   Solution: 10 min

10. If λ=4 per hour and μ=12 per hour in an (M/M/1):(4/FIFO) queueing system, find the probability that there is no customer in the system. If $\lambda=\mu$, what is the value of this probability?
    Solution: 81/121 ;1/5.

PART B

Reference : "Probability,Statistics and Queueing Theory"
- T. Veerarajan

1. The local one-person barber shop can accommodate a maximum of 5 people at a time(4 waiting and 1 getting hair cut). Customers arrive according to a Poisson distribution with mean 5 per hour. The barber cuts hair at an average rate of 4 per hour.(Exponential service time).
   (a) What percentage of time is the barber idle?
   (b) What fraction of the potential customers are turned away?
   (c) What is the expected number of customers waiting for a hair cut?
   (d) How much time can a customer expect to spend in the barber shop?(Page no: 506)

2. A bank has two tellers working on savings accounts. The first teller handles withdrawals only. The second teller handles deposits only. It has been found that the service time of 3 min per customer. Depositors are found to arrive in a Poisson fashion throughout the day with mean arrival rate of 16 per hour. Withdrawers also arrive in a Poisson fashion with mean arrival rate of 14 per hour. What would be the effect on the average waiting time for the customers if each teller could handle both withdrawals and deposits. What would be the effect, if this could only be accomplished by increasing the service time to 3.5 min.? (Page no: 500)

3. Customers arrive at a one-man barber shop according to a Poisson process mean interarrival time of 12 min. Customers spend an average of 10 min in the barber's chair.
   (a) What is the expected number of customers in the barber shop and in the queue?
   (b) Calculate the percentage of time an arrival can walk straight into the barber's chair without having to wait.
   © How much time can a customer expect to spend in the barber's shop?
   (e)Management will provide another chair and hire another barber, when a customer's waiting time in the shop exceeds 1.25h. How much must the average rate of arrivals increase to warrant a second barber?
   (f)What is the probability that the waiting time in the system is greater than 30 min?
   (page no: 490)

4. A 2-person barber shop has 5 chairs to accommodate waiting customers. Potential customers, who arrive when all 5 chairs are full, leave without entering barber shop. Customers arrive at the average rate of 4 per hour and spend an average of 12 min in the barber's chair. Compute P_0,P_1,$P_7E(N_q)$ and E(W).(page no:510)

5. Derive the difference equations for a Poisson queue system in the steady state.(page no:470)
6. There are 3 typists in an office. Each typist can type an average of 6 letters per hour. If letters arrive for being typed at the rate of 15 letters per hour.
   - What fraction of the time all the typists will be busy?
   - What is the average number of letters waiting to be typed?
   - What is the average time a letter has to spend for waiting and for being typed?
   - What is the probability that a letter will take longer than 20 min. waiting to be typed and being typed?

   Solution: Refer : Probability and Queueing Theory by G. Balaji pg.5.33.

7. Determine the steady state probabilities for M/M/C queueing system.

Solution: Refer : Probability and Queueing Theory by G. Balaji pg.5.52.

8. An automatic car wash facility operates with only one bay. Cars arrive according to a poisson distribution with a mean of 4 cars per hour and may wait in the facility's parking lot if the bay is busy. If the service time for all the cars is constant and equal to 10 minutes, determine
   - Mean number of customers in the system
   - Mean waiting time of a customer in the system
   - Mean waiting time of a customer in the queue
   - Mean number of customers in the queue

   Solution: Refer : Probability and Queueing Theory by G. Balaji pg.5.54.

UNIT V

NON MARKOVIAN QUEUES AND QUEUE NETWORKS

PART A

1. What is the probability then an arrival to an infinite capacity 3 server poisson queuing system with $\frac{\lambda}{\mu} = 2$ and P_o= 1/9 enters the service without waiting.

Solution: P(without waiting) = P(N<3)= $P_o+P_1+P_2$

$$P_n = \frac{1}{n!}\left(\frac{\lambda}{\mu}\right)^n P_o \quad when \quad n \le c = 3$$

$$P(N < 3) = \frac{1}{9} + \frac{2}{9} + \frac{1}{2} \times 2^2 \times \frac{1}{9} = \frac{5}{9}$$

2. Define Little's formula.

` Solution: (i) $E(N_s) = \frac{\lambda}{\mu - \lambda} = \lambda E(W_s)$

(ii) $E(N_q) = \frac{\lambda^2}{\mu(\mu - \lambda)} = \lambda E(W_q)$

(iii) $E(W_s) = E(W_q) + \frac{1}{\mu}$

(iv) $E(N_s) = E(N_q) + \frac{\lambda}{\mu}$

3. Write down the Pollaczek – khinchine formula.
`Solution: The average number of customers in the system is
$\frac{\lambda^2\sigma^2 + \rho^2}{2(1-\rho)} + \rho$

4. Define Pollaczek khinchine formula for average queue length.
Solution: Average queue length= $\frac{\lambda^2\sigma^2 + \rho^2}{2(1-\rho)}$

5. Define P-K formula for average waiting time of a customer in the queue.
Solution: Average waiting time of a customer in the queue =
$\frac{\lambda^2\sigma^2 + \rho^2}{2\lambda(1-\rho)}$

6. Define P-K formula for average waiting time that a customer spends in the system.
Solution: Average waiting time of a customer in the system =
$\frac{\lambda^2\sigma^2 + \rho^2}{2\lambda(1-\rho)} + \frac{1}{\mu}$

PART B

1. Derive the Balance equation of the birth and death process.
Solution: Refer : Probability and Queueing Theory by G. Balaji pg.4.88
2. Derive the Pollaczek- Khinchine formula.

Solution: Refer : Probability and Queueing Theory by G. Balaji pg.5.55.

3. Consider a single server, poisson input queue with mean arrival rate of 10 hour currently the server works according to an exponential distribution with mean service time of 5 minutes. Management has a training course which will result in an improvement in the variance of the service time but at a slight increase in the mean. After completion of the course;, it is estimated that the mean service time will increase to 5.5 minutes but the standard deviation will decrease from 5 minutes to 4 minutes. Management would like to know ;whether they should have the server undergo further training.

   Solution: Refer : Probability and Queueing Theory by G. Balaji pg.5.59.

4. In a heavy machine shop, the overhead crane is 75% utilized. Time study observations gave the average slinging time as 10.5 munutes with a standard deviation of 8.8 minutes. What is the average calling rate for the services of the crane and what is the average delay in getting service? If the average service time is cut to 8.0 minutes, with a standard deviation of 6.0 minutes, how much reduction will occur, on average, in the delay of getting served?

   Solution: Refer : Probability and Queueing Theory by G. Balaji pg.5.61.

5. Automatic car wash facility operates with only on Bay. Cars arrive according to a Poisson process, with mean of 4 cars per hour and may wait in the facility's parking lot if the bay is busy. If the service time for all cars is con;stant and equal to 10 min, determine L_s, L_q, W_s and W_q

   Solution: Refer : Probability and Queueing Theory by G. Balaji pg.5.64.

CS 2255 DATABASE MANAGEMENT SYSTEMS

(Common to CSE & IT)

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Text Books:

1. Abraham Silberschatz, Henry F. Korth, S. Sudharshan, “Database System Concepts”, Fifth Edition, Tata McGraw Hill, 2006 (Unit I and Unit-V) .
2. C.J.Date, A.Kannan, S.Swamynathan, “An Introduction to Database Systems”, Eighth Edition, Pearson Education, 2006.(Unit II, III and IV)

References:

1. Ramez Elmasri, Shamkant B. Navathe, “Fundamentals of Database Systems”, FourthEdition , Pearson / Addision wesley, 2007.
2. Raghu Ramakrishnan, “Database Management Systems”, Third Edition, McGraw Hill, 2003.
3. S.K.Singh, “Database Systems Concepts, Design and Applications”, First Edition, Pearson Education, 2006.

TWO MARKS

UNIT: 1
INTRODUCTION

1. Define database management system?

Database management system (DBMS) is a collection of interrelated data and a set of programs to access those data.

2. List any eight applications of DBMS.

a) Banking
b) Airlines
c) Universities
d) Credit card transactions
e) Tele communication
f) Finance
g) Sales
h) Manufacturing
) Human resources

3. What are the disadvantages of file processing system?

The disadvantages of file processing systems are

a) Data redundancy and inconsistency
b) Difficulty in accessing data
c) Data isolation
d) Integrity problems
e) Atomicity problems
f) Concurrent access anomalies

4. What are the advantages of using a DBMS?

The advantages of using a DBMS are

a) Controlling redundancy
b) Restricting unauthorized access
c) Providing multiple user interfaces
d) Enforcing integrity constraints.
e) Providing back up and recovery

5. Give the levels of data abstraction?

a) Physical level
b) logical level
c) view level

6. Define instance and schema?

Instance: Collection of data stored in the data base at a particular moment is

called an Instance of the database.

Schema: The overall design of the data base is called the data base schema.

7. Define the terms 1) physical schema 2) logical schema.

Physical schema: The physical schema describes the database design at the physical level, which is the lowest level of abstraction describing how the data are actually stored.

Logical schema: The logical schema describes the database design at the logical level, which describes what data are stored in the database and what relationship exists among the data.

8. What is conceptual schema?

The schemas at the view level are called subschemas that describe different views of the database.

9. Define data model?

A data model is a collection of conceptual tools for describing data, data relationships, data semantics and consistency constraints.

10. What is storage manager?

A storage manager is a program module that provides the interface between the low level data stored in a database and the application programs and queries submitted to the system.

11. What are the components of storage manager?

The storage manager components include

a) Authorization and integrity manager
b) Transaction manager
c) File manager
d) Buffer manager

12. What is the purpose of storage manager?

The storage manager is responsible for the following

a) Interaction with he file manager
b) Translation of DML commands in to low level file system commands
c) Storing, retrieving and updating data in the database

13. **List the data structures implemented by the storage manager**.

The storage manager implements the following data structure

a) Data files
b) Data dictionary
c) indices

14. What is a data dictionary?

A data dictionary is a data structure which stores meta data about the structure of

the database ie. the schema of the database.

15. What is an entity relationship model?

The entity relationship model is a collection of basic objects called entities and relationship among those objects. An entity is a thing or object in the real world that is distinguishable from other objects.

16. What are attributes? Give examples.

An entity is represented by a set of attributes. Attributes are descriptive properties possessed by each member of an entity set.

Example: possible attributes of customer entity are customer name, customer id, customer street, customer city.

17. What is relationship? Give examples

A relationship is an association among several entities.

Example: A depositor relationship associates a customer with each account that he/she has.

18. Define the terms i) Entity set ii) Relationship set

Entity set: The set of all entities of the same type is termed as an entity set.

Relationship set: The set of all relationships of the same type is termed as a relationship set.

19. Define single valued and multivalued attributes.

Single valued attributes: attributes with a single value for a particular entity are called single valued attributes.

Multivalued attributes: Attributes with a set of value for a particular entity are called multivalued attributes.

20. What are stored and derived attributes?

Stored attributes: The attributes stored in a data base are called stored attributes.

Derived attributes: The attributes that are derived from the stored attributes are called derived attributes.

21. What are composite attributes?

Composite attributes can be divided in to sub parts.

22. Define null values.

In some cases a particular entity may not have an applicable value for an attribute or if we do not know the value of an attribute for a particular entity. In these cases null value is used.

23. Define the terms i) Entity type ii) Entity set

Entity type: An entity type defines a collection of entities that have the same attributes.

Entity set: The set of all entities of the same type is termed as an entity set.

24. What is meant by the degree of relationship set?

The degree of relationship type is the number of participating entity types.

25. Define the terms i) Key attribute ii) Value set

Key attribute: An entity type usually has an attribute whose values are distinct from each individual entity in the collection. Such an attribute is called a key attribute.

Value set: Each simple attribute of an entity type is associated with a value set that specifies the set of values that may be assigned to that attribute for each individual entity.

26. Define weak and strong entity sets?

Weak entity set: entity set that do not have key attribute of their own are called weak entity sets.

Strong entity set: Entity set that has a primary key is termed a strong entity set.

27. What does the cardinality ratio specify?

Mapping cardinalities or cardinality ratios express the number of entities to which another entity can be associated. Mapping cardinalities must be one of the following:

- One to one
- One to many
- Many to one
- Many to many

28. Explain the two types of participation constraint.

1. **Total:** The participation of an entity set E in a relationship set R is said to be **total** if every entity in E participates in at least one relationship in R.
2. **Partial:** if only some entities in E participate in relationships in R, the participation of entity set E in relationship R is said to be **partial.**

29. Define the terms i) DDL ii) DML

DDL: Data base schema is specified by a set of definitions expressed by a special language called a data definition language.

DML: A data manipulation language is a language that enables users to access or manipulate data as organized by the appropriate data model.

30. Write short notes on relational model

The relational model uses a collection of tables to represent both data and the relationships among those data. The relational model is an example of a record based model.

31. Define tuple and attribute

Attributes: column headers

Tuple: Row

32. **Define the term relation**.

Relation is a subset of a Cartesian product of list domains.

33. Define tuple variable

Tuple variable is a variable whose domain is the set of all tuples.

34. Define the term Domain.

For each attribute there is a set of permitted values called the ***domain*** of that attribute.

35. What is a candidate key?

Minimal super keys are called ***candidate keys.***

36. What is a primary key?

Primary key is chosen by the database designer as the principal means of identifying an entity in the entity set.

37. What is a super key?

A ***super key*** is a set of one or more attributes that collectively allows us to identify uniquely an entity in the entity set.

38. Define- relational algebra.

The relational algebra is a procedural query language. It consists of a set of operations that take one or two relation as input and produce a new relation as output.

39. What is a SELECT operation?

The ***select*** operation selects tuples that satisfy a given predicate. We use the lowercase letter σ to denote selection.

40. What is a PROJECT operation?

The project operation is a unary operation that returns its argument relation with certain attributes left out. Projection is denoted by pie (π)**.**

41. Write short notes on tuple relational calculus.

The tuple relational calculation is anon procedural query language. It describes the desired information with out giving a specific procedure for obtaining that information.

A query or expression can be expressed in tuple relational calculus as

$\{t \mid P(t)\}$

which means the set of all tuples't' such that predicate P is true for 't'.

Notations used:

- $t[A] \rightarrow$ the value of tuple 't' on attribute, A
- $t \in r \rightarrow$ tuple 't' is in relation 'r'
- $\exists \rightarrow$ there exists
    - Definition for 'there exists' ($\exists$):
    - $\exists\, t \in r(Q(t))$

- which means there exists a tuple 't' in relation 'r' such that predicate Q(t) is true.

- $\forall \rightarrow$ for all
  - Definition for 'for all' ($\forall$):
  - $\forall t \in r(Q(t))$
  - which means Q(t) is true for all tuples 't' in relation 'r'.
- $\_ \rightarrow$ Implication

  Definition for Implication ($\_$):

  P$_$Q means if P is true then Q must be true.

42. Write short notes on domain relational calculus

The domain relational calculus uses domain variables that take on values from an attribute domain rather than values for entire tuple.

43. Define query language?

A query is a statement requesting the retrieval of information. The portion of DML that involves information retrieval is called a query language.

44. Write short notes on Schema diagram.

A database schema along with primary key and foreign key dependencies can be depicted pictorially by schema diagram. Each relation appears as a box with attributes listed inside it and the relation name above it.

45. What is foreign key?

A relation schema r1 derived from an ER schema may include among its attributes the primary key of another relation schema r2.this attribute is called a ***foreign key*** from r1 referencing r2.

UNIT: 2
RELATIONAL MODEL

1. What are the parts of SQL language?

The SQL language has several parts:

- data - definitition language
- Data manipulation language
- View definition
- Transaction control
- Embedded SQL
- Integrity
- Authorization

2. What are the categories of SQL command?

SQL commands are divided in to the following categories:

1. Data - Definitition Language
2. Data Manipulation language

3. Data Query Language
4. Data Control Language
5. Data Administration Statements
6. Transaction Control Statements

3. What are the three classes of SQL expression?

SQL expression consists of three clauses:

- Select
- From
- Where

4. Give the general form of SQL query?

Select A_1, A_2……., An
From R_1, R_2……, R_m
Where P

5. What is the use of rename operation?

Rename operation is used to rename both relations and a attributes.
It uses the as clause, taking the form:

Old-name **as** new-name

6. Define tuple variable?

Tuple variables are used for comparing two tuples in the same relation. The tuple variables are defined in the **from** clause by way of the **as** clause.

7. List the string operations supported by SQL?

1) Pattern matching Operation
2) Concatenation
3) Extracting character strings
4) Converting between uppercase and lower case letters.

8. List the set operations of SQL?

1) Union
2) Intersect operation
3) The except operation

9. What is the use of Union and intersection operation?

Union: The result of this operation includes all tuples that are either in r1 or in r2 or in both r1 and r2.Duplicate tuples are automatically eliminated.
Intersection: The result of this relation includes all tuples that are in both r1 and r2.

10. What are aggregate functions? And list the aggregate functions supported by SQL?

Aggregate functions are functions that take a collection of values as input and return a single value.

Aggregate functions supported by SQL are

- Average: avg
- Minimum: min
- Maximum: max
- Total: sum
- Count: count

11. What is the use of group by clause?

Group by clause is used to apply aggregate functions to a set of tuples. The attributes given in the **group by** clause are used to form groups. Tuples with the same value on all attributes in the **group by** clause are placed in one group.

12. What is the use of sub queries?

A sub query is a select-from-where expression that is nested with in another query. A common use of sub queries is to perform tests for set membership, make set comparisions, and determine set cardinality.

13. What is view in SQL? How is it defined?

Any relation that is not part of the logical model, but is made visible to a user as a virtual relation is called a view.

We define view in SQL by using the **create view** command. The form of the **create view** command is

Create view v as <query expression>

14. What is the use of with clause in SQL?

The **with** clause provides a way of defining a temporary view whose definition is available only to the query in which the **with** clause occurs.

15. List the table modification commands in SQL?

- Deletion
- Insertion
- Updates
- Update of a view

16. List out the statements associated with a database transaction?

- Commit work
- Rollback work

17. What is transaction?

Transaction is a unit of program execution that accesses and possibly updated various data items.

18. List the SQL domain Types?

SQL supports the following domain types.

1) Char(n) 2) varchar(n) 3) int 4) numeric(p,d) 5) float(n) 6) date.

19. What is the use of integrity constraints?

Integrity constraints ensure that changes made to the database by authorized users do not result in a loss of data consistency. Thus integrity constraints guard against accidental damage to the database.

20. Mention the 2 forms of integrity constraints in ER model?

- Key declarations
- Form of a relationship

21. What is trigger?

Triggers are statements that are executed automatically by the system as the side effect of a modification to the database.

22. What are domain constraints?

A domain is a set of values that may be assigned to an attribute .all values that appear in a column of a relation must be taken from the same domain.

23. What are referential integrity constraints?

A value that appears in one relation for a given set of attributes also appears for a certain set of attributes in another relation.

24. What is assertion? Mention the forms available.

An assertion is a predicate expressing a condition that we wish the database always to satisfy.

- Domain integrity constraints.
- Referential integrity constraints

25. Give the syntax of assertion?

Create assertion <assertion name>**check**<predicate>

26. What is the need for triggers?

Triggers are useful mechanisms for alerting humans or for starting certain tasks automatically when certain conditions are met.

27. List the requirements needed to design a trigger.

The requirements are

- Specifying when a trigger is to be executed.
- Specify the actions to be taken when the trigger executes.

28. Give the forms of triggers?

- The triggering event can be insert or delete.
- For updated the trigger can specify columns.
- The referencing old row as clause
- The referencing new row as clause
- The triggers can be initiated before the event or after the event.

29. What does database security refer to?

Database security refers to the protection from unauthorized access and malicious destruction or alteration.

30. List some security violations (or) name any forms of malicious access.

- Unauthorized reading of data
- Unauthorized modification of data
- Unauthorized destruction of data.

31. List the types of authorization.

- Read authorization
- Write authorization
- Update authorization
- Drop authorization

32. What is authorization graph?

Passing of authorization from one user to another can be represented by an authorization graph.

33. List out various user authorization to modify the database schema.

- Index authorization
- Resource authorization
- Alteration authorization
- Drop authorization

34. What are audit trails?

An audit trail is a log of all changes to the database along with information such as which user performed the change and when the change was performed.

35. Mention the various levels in security measures.

- Database system
- Operating system
- Network
- Physical
- Human

36. Name the various privileges in SQL?

- Delete
- Select
- Insert
- Update

37. Mention the various user privileges.

- All privileges directly granted to the user or role.
- All privileges granted to roles that have been granted to the user or role.

38. Give the limitations of SQL authorization.

- The code for checking authorization becomes intermixed with the rest of the application code.
- Implementing authorization through application code rather than specifying it declaratively in SQL makes it hard to ensure the absence of loopholes.

39. Give some encryption techniques?

- DES
- AES
- Public key encryption

40. What does authentication refer?

Authentication refers to the task of verifying the identity of a person.

41. List some authentication techniques.

- Challenge response scheme
- Digital signatures
- Nonrepudiation

42. Define Boyce codd normal form

A relation schema R is in BCNF with respect to a set F of functional dependencies if, for all functional dependencies in F^+ of the form.$\alpha \rightarrow \beta$.

43. List the disadvantages of relational database system

- Repetition of data
- Inability to represent certain information.

44. What is first normal form?

The domain of attribute must include only atomic (simple, indivisible) values.

45. What is meant by functional dependencies?

Consider a relation schema R and $\alpha \subseteq R$ and $\beta \subseteq R$. The functional dependency $\alpha \rightarrow \beta$ holds on relational schema R if in any legal relation r(R), for all pairs of tuples t1 and t2 in r such that t1 [α] =t2 [α], and also t1 [β] =t2 [β].

46. What are the uses of functional dependencies?

- To test relations to see whether they are legal under a given set of functional dependencies.
- To specify constraints on the set of legal relations.

47. Explain trivial dependency?

Functional dependency of the form $\alpha \rightarrow \beta$. is trivial if $\alpha \subseteq \beta$. Trivial functional dependencies are satisfied by all the relations.

48. What are axioms?

Axioms or rules of inference provide a simpler technique for reasoning about

functional dependencies.

49. What is meant by computing the closure of a set of functional dependency?

The closure of F denoted by F^+ is the set of functional dependencies logically implied by F.

50. What is meant by normalization of data?

It is a process of analyzing the given relation schemas based on their Functional Dependencies (FDs) and primary key to achieve the properties

- Minimizing redundancy
- Minimizing insertion, deletion and updating anomalies.

51. Define canonical cover?

A canonical cover F_c for F is a set of dependencies such that F logically implies all dependencies in F_C and F_c logically implies all dependencies in F. F_c must have the following properties.

52. List the properties of canonical cover.

F_c must have the following properties.

- No functional dependency in F_c contains an extraneous attribute.
- Each left side of a functional dependency in F_c is unique.

53. Explain the desirable properties of decomposition.

- Lossless-join decomposition
- Dependency preservation
- Repetition of information

54. What is 2NF?

A relation schema R is in 2NF if it is in 1NF and every non-prime attribute A in R is fully functionally dependent on primary key.

UNIT: 3
DATABASE DESIGN

1. What is an index?

An index is a structure that helps to locate desired records of a relation quickly, without examining all records.

2. Define query optimization.

Query optimization refers to the process of finding the lowest –cost method of evaluating a given query.

3. What are called jukebox systems?

Jukebox systems contain a few drives and numerous disks that can be loaded into one of the drives automatically.

4. What are the types of storage devices?

- Primary storage
- Secondary storage
- Tertiary storage
- Volatile storage
- Nonvolatile storage

5. What is called remapping of bad sectors?

If the controller detects that a sector is damaged when the disk is initially formatted, or when an attempt is made to write the sector, it can logically map the sector to a different physical location.

6. Define access time.

Access time is the time from when a read or write request is issued to when data transfer begins.

7. Define seek time.

The time for repositioning the arm is called the seek time and it increases with the distance that the arm is called the seek time.

8. Define average seek time.

The average seek time is the average of the seek times, measured over a sequence of random requests.

9. Define rotational latency time.

The time spent waiting for the sector to be accessed to appear under the head is called the rotational latency time.

10. Define average latency time.

The average latency time of the disk is one-half the time for a full rotation of the disk.

11. What is meant by data-transfer rate?

The data-transfer rate is the rate at which data can be retrieved from or stored to the disk.

12. What is meant by mean time to failure?

The mean time to failure is the amount of time that the system could run continuously without failure.

13. What is a block and a block number?

A block is a contiguous sequence of sectors from a single track of one platter. Each request specifies the address on the disk to be referenced. That address is in the form of a block number.

14. What are called journaling file systems?

File systems that support log disks are called journaling file systems.

15. What is the use of RAID?

A variety of disk-organization techniques, collectively called redundant arrays of independent disks are used to improve the performance and reliability.

16. What is called mirroring?

The simplest approach to introducing redundancy is to duplicate every disk. This technique is called mirroring or shadowing.

17. What is called mean time to repair?

The mean time to failure is the time it takes to replace a failed disk and to restore the data on it.

18. What is called bit-level striping?

Data striping consists of splitting the bits of each byte across multiple disks. This is called bit-level striping.

19. What is called block-level striping?

Block level striping stripes blocks across multiple disks. It treats the array of disks as a large disk, and gives blocks logical numbers

.

20. What are the two main goals of parallelism?

- Load –balance multiple small accesses, so that the throughput of such accesses increases.
- Parallelize large accesses so that the response time of large accesses is reduced

.

21. What are the factors to be taken into account when choosing a RAID level?

- Monetary cost of extra disk storage requirements.
- Performance requirements in terms of number of I/O operations
- Performance when a disk has failed.
- Performances during rebuild.

22. What is meant by software and hardware RAID systems?

RAID can be implemented with no change at the hardware level, using only software modification. Such RAID implementations are called software RAID systems and the systems with special hardware support are called hardware RAID systems.

23. Define hot swapping?

Hot swapping permits the removal of faulty disks and replaces it by new ones without turning power off. Hot swapping reduces the mean time to repair.

24. What are the ways in which the variable-length records arise in database systems?

- Storage of multiple record types in a file.
- Record types that allow variable lengths for one or more fields.
- Record types that allow repeating fields.

25. What is the use of a slotted-page structure and what is the information present in the header?

The slotted-page structure is used for organizing records within a single block. The header contains the following information.

- The number of record entries in the header.
- The end of free space
- An array whose entries contain the location and size of each record.

26. What are the two types of blocks in the fixed –length representation? Define them.

- Anchor block: Contains the first record of a chain.
- Overflow block: Contains the records other than those that are the first record of a chain.

27. What is known as heap file organization?

In the heap file organization, any record can be placed anywhere in the file where there is space for the record. There is no ordering of records. There is a single file for each relation.

28. What is known as sequential file organization?

In the sequential file organization, the records are stored in sequential order, according to the value of a "search key" of each record.

29. What is hashing file organization?

In the hashing file organization, a hash function is computed on some attribute of each record. The result of the hash function specifies in which block of the file the record hould be placed.

30. What is known as clustering file organization?

In the clustering file organization, records of several different relations are stored in the same file.

31. What are the types of indices?

- Ordered indices
- Hash indices

32. What are the techniques to be evaluated for both ordered indexing and hashing?

- Access types
- Access time

- Insertion time
- Deletion time
- Space overhead

33. What is known as a search key?

An attribute or set of attributes used to look up records in a file is called a search key.

34. What is a primary index?

A primary index is an index whose search key also defines the sequential order of the file.

35. What are called index-sequential files?

The files that are ordered sequentially with a primary index on the search key, are called index-sequential files.

36. What are the two types of indices?

- Dense index
- Sparse index

37. What are called multilevel indices?

Indices with two or more levels are called multilevel indices.

38. What is B-Tree?

A B-tree eliminates the redundant storage of search-key values .It allows search key values to appear only once.

39. What is a B+-Tree index?

A B+-Tree index takes the form of a balanced tree in which every path from the root of the root of the root of the tree to a leaf of the tree is of the same length.

40. What is a hash index?

A hash index organizes the search keys, with their associated pointers, into a hash file structure.

41. What is called query processing?

Query processing refers to the range of activities involved in extracting data from a database.

42. What are the steps involved in query processing?

The basic steps are:

- parsing and translation
- optimization
- Evaluation

43. What is called an evaluation primitive?

A relational algebra operation annotated with instructions on how to evaluate is

called an evaluation primitive.

44. What is called a query evaluation plan?

A sequence of primitive operations that can be used to evaluate a query is a query evaluation plan or a query execution plan.

45. What is called a query –execution engine?

The query execution engine takes a query evaluation plan, executes that plan, and returns the answers to the query.

46. What are called as index scans?

Search algorithms that use an index are referred to as index scans.

47. What is called as external sorting?

Sorting of relations that do not fit into memory is called as external sorting.

48. What is called as recursive partitioning?

The system repeats the splitting of the input until each partition of the build input fits in the memory. Such partitioning is called recursive partitioning.

49. What is called as an N-way merge?

The merge operation is a generalization of the two-way merge used by the standard in-memory sort-merge algorithm. It merges N runs, so it is called an N-way merge.

50. What is known as fudge factor?

The number of partitions is increased by a small value called the fudge factor, which is usually 20 percent of the number of hash partitions computed.

UNIT: 4
TRANSACTIONS

1. What is transaction?

Collections of operations that form a single logical unit of work are called transactions.

2. What are the two statements regarding transaction?

The two statements regarding transaction of the form:

- Begin transaction
- End transaction

3. What are the properties of transaction?

The properties of transactions are:

- Atomicity
- Consistency
- Isolation

- Durability

4. What is recovery management component?

Ensuring durability is the responsibility of a software component of the base system called the recovery management component.

5. When is a transaction rolled back?

Any changes that the aborted transaction made to the database must be undone. Once the changes caused by an aborted transaction have been undone, then the transaction has been rolled back.

6. What are the states of transaction?

The states of transaction are

- Active
- Partially committed
- Failed
- Aborted
- Committed
- Terminated

7. What is a shadow copy scheme?

It is simple, but efficient, scheme called the shadow copy schemes. It is based on making copies of the database called shadow copies that one transaction is active at a time. The scheme also assumes that the database is simply a file on disk.

8. Give the reasons for allowing concurrency?

The reasons for allowing concurrency is if the transactions run serially, a short transaction may have to wait for a preceding long transaction to complete, which can lead to unpredictable delays in running a transaction. So concurrent execution reduces the unpredictable delays in running transactions.

9. What is average response time?

The average response time is that the average time for a transaction to be completed after it has been submitted.

10. What are the two types of serializability?

The two types of serializability is

- Conflict serializability
- View serializability

11. Define lock?

Lock is the most common used to implement the requirement is to allow a transaction to access a data item only if it is currently holding a lock on that item.

12. What are the different modes of lock?

The modes of lock are:

- Shared
- Exclusive

13. Define deadlock?

Neither of the transaction can ever proceed with its normal execution. This situation is called deadlock.

14. Define the phases of two phase locking protocol

- Growing phase: a transaction may obtain locks but not release any lock.
- Shrinking phase: a transaction may release locks but may not obtain any new locks.

15. Define upgrade and downgrade?

It provides a mechanism for conversion from shared lock to exclusive lock is known as upgrade.

It provides a mechanism for conversion from exclusive lock to shared lock is known as downgrade.

16. What is a database graph?

The partial ordering implies that the set D may now be viewed as a directed acyclic graph, called a database graph.

17. What are the two methods for dealing deadlock problem?

The two methods for dealing deadlock problem is deadlock detection and deadlock recovery.

18. What is a recovery scheme?

An integral part of a database system is a recovery scheme that can restore the database to the consistent state that existed before the failure.

19. What are the two types of errors?

The two types of errors are:

- Logical error
- System error

20. What are the storage types?

The storage types are:

- Volatile storage
- Nonvolatile storage

21. Define blocks?

The database system resides permanently on nonvolatile storage, and is into fixed-length storage units called blocks.

22. What is meant by Physical blocks?

The input and output operations are done in block units. The blocks residing on

the disk are referred to as physical blocks.

23. What is meant by buffer blocks?

The blocks residing temporarily in main memory are referred to as buffer blocks.

24. What is meant by disk buffer?

The area of memory where blocks reside temporarily is called the disk buffer.

25. What is meant by log-based recovery?

The most widely used structures for recording database modifications is the log. The log is a sequence of log records, recording all the update activities in the database. There are several types of log records.

26. What are uncommitted modifications?

The immediate-modification technique allows database modifications to be output to the database while the transaction is still in the active state. Data modifications written by active transactions are called uncommitted modifications.

27. Define shadow paging.

An alternative to log-based crash recovery technique is shadow paging. This technique needs fewer disk accesses than do the log-based methods.

28. Define page.

The database is partitioned into some number of fixed-length blocks, which are referred to as pages.

29. Explain current page table and shadow page table.

The key idea behind the shadow paging technique is to maintain two page tables during the life of the transaction: the current page table and the shadow page table. Both the page tables are identical when the transaction starts. The current page table may be changed when a transaction performs a write operation.

30. What are the drawbacks of shadow-paging technique?

- Commit Overhead
- Data fragmentation
- Garbage collection

30. Define garbage collection.

Garbage may be created also as a side effect of crashes. Periodically, it is necessary to find all the garbage pages and to add them to the list of free pages. This process is called garbage collection.

32. Differentiate strict two phase locking protocol and rigorous two phase locking protocol.

In **strict two phase locking protocol** all exclusive mode locks taken by a transaction is held until that transaction commits.

Rigorous two phase locking protocol requires that all locks be held until the transaction commits.

33. How the time stamps are implemented

- Use the value of the system clock as the time stamp. That is a transaction's time stamp is equal to the value of the clock when the transaction enters the system.
- Use a logical counter that is incremented after a new timestamp has been assigned; that is the time stamp is equal to the value of the counter.

34. What are the time stamps associated with each data item?

- W-timestamp (Q) denotes the largest time stamp if any transaction that executed WRITE (Q) successfully.
- R-timestamp (Q) denotes the largest time stamp if any transaction that executed READ (Q) successfully.

UNIT: 5
IMPLEMENTATION TECHNIQUES

1. What is meant by object-oriented data model?

The object-oriented paradigm is based on encapsulation of data and code related to an object in to a single unit, whose contents are not visible to the outside world.

2. What is the major advantage of object-oriented programming paradigm?

The ability to modify the definition of an object without affecting the rest of the system is the major advantage of object-oriented programming paradigm.

3. What are the methods used in object-oriented programming paradigm?

- read-only
- update

4. What is the main difference between read-only and update methods?

A read-only method does not affect the values of a variable in an object, whereas an update method may change the values of the variables.

5. What is the use of keyword ISA?

The use of keyword ISA is to indicate that a class is a specialization of another class.

6. Differentiate sub-class and super-class?

The specialization of a class is called subclasses.eg: employee is a subclass of person and teller is a subclass of employee.Conversely, employee is a super class of teller, and person is a super class of employee.

7. What is substitutability?

Any method of a class-say A can equally well be invoked with any object belonging to any subclasses B of A. This characteristic leads to code reuse, since the messages, methods, and functions do not have to be written again for objects of class B.

8. What is multiple inheritance?

Multiple inheritance permits a class to inherit variables and methods from multiple super classes.

9. What is DAG?

The class-subclass relationship is represented by a directed acyclic graph.eg: employees can be temporary or permanenet.we may create subclasses temporary and permanenet, of the class employee.

10. What is disadvantage of multiple inheritance?

There is potential ambiguity if the same variable or method can be inherited from more than one superclass.eg: student class may have a variable dept identifying a student's department, and the teacher class may correspondingly have a variable dept identifying a teacher's department.

11. What is object identity?

An object retains its identity even if some or all the values of variables or definitions of methods change overtime.

12. What are the several forms of identity?

- Value
- Name
- Built-in

13. What is a value?

A data value is used for identity. This form of identity is used in relational systems.eg: The primary key value of a tuple identifies the tuple.

14. What is a Name?

A user-supplied name is used for identity. This form of identity is used for files in file systems. The user gives each file a name that uniquely identifies it, regardless of its contents.

15What is a Built-in

A notation of identity is built-into the data model or programming language and no user-supplied identifier is required. This form of identity is used in objectoriented systems.

16 What is meant by object identifiers?

Object-oriented systems use an object identifier to identify objects. Object identifiers are unique: that is each object has a single identifier, and no two objects have the same identifier.

17. What are composite objects?

Objects that contain other objects are called complex objects or composite objects.

18. What is object containment?

References between objects can be used to model different real-world concepts.

19. Why containment is important in oosystems?

Containment is an important concept in oosystems because it allows different users to view data at different granularities.

20. Define object-relational systems?

Systems that provide object-oriented extensions to relational systems are called object-relational systems.

21. How persistent programming languages differ from traditional programming languages?

Database languages differ from traditional programming languages in that they directly manipulate data that are persistent-that is, data that continue to exist even after the program terminated. Relation in a database and tuples in a relation are examples of persistent data. In contrast, the only persistent data that traditional programming languages directly manipulate are files.

22. Define atomic domains?

A domain is atomic if elements of the domain are considered to be indivisible units.

23. Define 1NF?

First normal form is one which requires that all attributes have atomic domains.

24. What is nested relational model?

The nested relational model is an extension of relational model in which domains may be either atomic or relation valued.

25. List some instances of collection types?

- sets
- arrays
- multisets

26. How to create values of structured type?

Constructor functions are used to create values of structured types. A function with the same name as a structured type is a constructor function for the structured type.

27. Write a query to define tables students and teachers as sub tables of people?

Create table students of student under people
Create table teachers of teacher under people

28. What is a homogeneous distributed database?

In homogeneous distributed databases, all sites have identical database management system software, are aware of one another, and agree to cooperate in processing user's requests.

29. What is a heterogeneous distributed database?

In a heterogeneous distributed database, different sites may use different schemas, and different dbms s/w.The sites may not be aware of one another, and they may provide only limited facilities for cooperation in transaction processing.

30. What are the two approaches to store relations in distributed database?

- Replication
- Fragmentation

31. What are the two different schemes for fragmenting a relation?

- horizontal
- vertical

32. What is horizontal fragmentation?

Horizontal fragmentation splits the relation by assuming each tuple of r to one or more fragments.

33. What is vertical fragmentation?

Vertical fragmentation splits the relation by decomposing the scheme R of relation r.

34. What are the various forms of data transparency?

- fragmentation transparency
- replication transparency
- location transparency

35. Define decision tree classifiers?

As the name suggests decision tree classifiers use a tree: each leaf node has an associated class, and each internal node has a predicate associated with it.

16 MARK QUESTIONS

UNIT: 1

1. EXPLAIN ABOUT DATABASE SYSTEM STRUCTURE?

Storage manager

- Authorization and integrity manager
- Transaction manager
- File manager
- Buffer manager

Storage manager implements several data structure as a part of physical system implementation

- Data function
- Data dictionary
- Indices

The query processor

- DDL interpreter
- DML
- Query evaluation engine

2. DESCRIBE RELATIONAL MODEL?

Structure of relational data base

- Basic structure
- Database schema
- Keys
- Schema diagram
- Query languages

3. BRIEFLY EXPLAIN RELATIONAL ALGEBRA?

Fundamental operations

- Unary operations
- Binary operations

Select operations

$\sigma_{branchname='perryridge'}(loan)$

The project operation∏

$\pi_{loannumber,amount}(loan)$

Composition of relational operations

- Relational algebra expressions

Union operations

r _ s

r and s must be a same arity.

They must have the same no of attributes.

The set difference operations

r-s produce a relation containing those tuples in r but not in s.

The Cartesian product operations

The rename operations

4. WHAT IS DATA MODELS? EXPLAIN IT DETAIL?

Entity relationship model

- Rectangles
- Ellipse
- Diamonds
- Lines

Relational model

Relational model use a collection of tables to represent both data and the relationships among those data. Each table has a multiple columns and each columns has unique name

Other data models

- Object oriented data model
- Object relational data model
- Network data model
- Hierarchical data model

5. BRIEFLY DESCRIBE RELATIONAL CALCULUS?WITH SOME EXAMPLES?

The tuple relational calculus

A query in a tuple relational calculus is expressed as

{t| P(t)}

- Example Queries
- Formal definition
- Safety of expressions
- Expressive power of languages

The domain relational calculus

- Example Queries
- Formal definition
- Safety of expressions
- Expressive power of languages

UNIT-2

1. DESCRIBE INTEGRITY AND SECURITY?

- **Domain constraint**
- **Referential integrity**

  A value that appears in one relation for a given set of attributes also appear for a certain set of attributes in another relation. This condition is called referential integrity.
- **Referential integrity and E-R models**
- **Database modification**
- **Referential integrity in SQL**

2. WHAT IS AGGREGATE FUNCTION?BRIEFLY DESCRIBE IT?

Aggregate functions are functions that take a collection of values as input and return a single value. SQL offers 5 built-in aggregate functions:

- Average: **avg**
- Minimum:**min**
- Maximum: **max**
- Total:**sum**
- Count:**count**

Average: **avg**

Select avg (balance)
From account
Where branch-name=’**perryridge**’

Count :**count**

select branch-name,**count(**distinct customer-name**)**
from depositior,account
where depositor.account-number=account.account-number
groupby branch-name

3. WHAT IS DATA DEFINITION LANGUAGE?EXPLAIN IT IN DETAIL?

The SQL DDL allows specification of not only a set of relations, but also

information after each relation, including

- The schema for each relation
- The domain of values associated with each attribute
- The integrity constraints
- The set of indices to be maintained for each relation
- The security and authorization information for each relation
- The physical storage structure of each relation on disk

Domain Types in SQL

Char(n),
varchar(n), int, small int, numeric(p,d), real, double, precision,
f loat(n), date, time, timestamp.

Schema Definition in SQL

- Primary key
- Check

4. EXPLAIN MECHANISM OF NESTED QUERIES?

SQL provides a mechanism for nesting subqueries.A subquery is a select from where expression that is nested within another query. A common use of sub queries is to perform tests for set membership, make set comparisons, and determine set cardinality.

- **Set membership**
  (select customer-name
  from depositor)
- **Set comparison**
  select distinct T.branch-name
  from branch as T,branch as S
  where T.assets > S.assets **and** S.branch-city='Brooklyn'
- **Test for Empty Relations**
  Select customer-name
  from borrower
  where exits (select *
  from depositor
  where depositor.customername=borrower.customer-name)
- **Test for the Absence of Duplicate Tuples**

5. WRITE SHORT NOTES ON MODIFICTION OF THE DATA BASE?

- **Definition**
  delete from r
  where P
- **Insertion**
  insert into account
  values ('A-9732','perryridge',1200)
- **Updates**
  update account
  s**et** balance=balance*1.05

- **Update of a view**
- **Transaction**

UNIT-3

1. DESCRIBE FILE ORGANISATION?

A file is organized logically as a sequence of records. These records are mapped onto disk blocks.

- **Fixed-Length Records**

  Type deposit=**record**
  Accountnumber:char(10);
  branch name:char(22);
  balance: real;
  end

- **Variable length records**
  - storage of multiple record types in a file
  - Record types that allow variable lengths for one or more fields
  - Record types that allow repeating fields
    - Byte string Representation
    - Fixed length representation
      - Reserved space
      - List representation

2. DEFINE RAID? BRIEFLY EXPLAIN IT?

A variety of disk organization techniques, collectively called redundant arrays of independent disks (RAID)

- Improvement of reliability via redundancy.
- Improvement in performance via parallelism
  1. Bit level striping
  2. Block level striping

RAID levels

- RAID level 0
- RAID level 1
- RAID level 2(memory style error correcting code)
- RAID level 3 (Bit interleaved parity organization)
- RAID level 4 (Block interleaved parity organization)
- RAID level 5 (Block interleaved distributed parity)
- RAID level 6 (P+Q redundancy)

3. WRITE SHORT NOTES ON INDEX STRUCTURE OF FILES?

There are two basic kinds of indices

1. **Ordered indices**
2. **Hash indices**

Each technique must be evaluated on the basis of these factors:

- **Access types**
- **Access time**
- **Insertion time**
- **Deletion time**
- **Space overhead**
  - **Ordered indices**
  - **Primary index**
  - **Dense and sparse indices**
  - **Multilevel index**
  - **Index update**
  - **Secondary indices**

B+-Tree index files

B+-Tree index structure is the most widely used of several index structures that maintain there efficiency despite insertion and deletion of data.

- **Structure of B+-Tree**
- **Queries on B+-Tree**
- **Update on B+-Tree**
- **B+-Tree file organization**
- **B-Tree index files**

4. EXPLAIN HASH FILE ORGANIZATION?

Hash functions

- **The distribution is uniform**

Hash functions assign each bucket the same number of search –key values from the set of all possible search-key values

- **The distributed in random**

In the average case each bucket will have nearly same no of values assigned to it, regardless of the actual distribution of search-key values

Handling of bucket overflows

- **Insufficient buckets**
- **Skew**

Open hashing

Under an alternative approach called open hashing

Close hashing

The form of hash structure that we have just described is something referred to as close hashing.

Hash indices

5. WHAT IS MAGNETIC DISKS?EXPLAIN IT?

Magnetic disk provides the bulk of secondary storage of modern computer

system. The disk capacity is growing at over 50% per year. But the storage requirements of large applications has also been growing very fast and in some case every faster than the growth rate of disk capacities**.** A large data base may require 100 of disks.

- Physical characteristics of disk

Physical disks are relatively simple. Each disc platter has a flat circular shape

We can call magnetic disk as

- **hard disk**
- **Floppy disk**

The read write head store information on a sector magnetically as reversals of the direction of magnetization of the magnetic material. There may be hundreds of concentric tracks on a disc surface, containing thousands of sectors.

Unit 4

1. DESCRIBE LOG BASED RECOVERY

The most usably structure for recording data base modification is the LOG

the log is a sequence of log records recording all the update activities in the data base. There are several types of log records. An update log records describes a single data base write it has these fields

- **Transaction identifier**
- **Data item identifier**
- **Old value**
- **New value**

The various types log records as.

- < T_i start >. Transaction T_i has started
- < T_i , T_x v_1,v_2 > .Transaction T_i has performed a right on data item
- < T_i commit > Transaction T_i has committed
- < T_i about > Transaction T_i has aborted
  - **Deferred data base modification**
  - **Immediate data base modification**
  - **Check point**
  - **Shadow paging**

2. WHAT IS SERIALIZABILITY?EXPLAIN ITS TYPES?

The data base system must control concurrent execution of transactions, to ensure that the data base state remains consistent. There are different forms of schedule equivalence they lead to the notions of

- Conflict serializability
- View serializability

Conflict serializability

We say that i_i and I_j conflict if they are operations by different transaction on the same data item and at least one of these instruction is a write operations

View serializability

The concept of view equivalence leads to the concept of View serializability we say that a schedules S is view serializable if it is view equivalent to a serial scheduler

3.WRITE SHORT NOTES ON TRANSACTION STATE?

A transaction may not always complete its execution successfully such a transaction is termed aborted

A transaction must be in one of the following states

- Active
- Partially committed
- Failed
- Aborted
- Committed

4. BRIEFLY DESCRIBE CONCURRENCYEXECUTION?

- Lock – based protocols
- Locks

There are various modes in which a data item may be locked in this section we restrict our attention to two modes

- Shared
- Exclusive

T_1 : lock – x(B);
read(B);
B:=B-50;
write(B);
unlock(B);
Lock-x(A);
read(A);
A:=A+50;
write(A);
unlock(A**).**

5. EXPLAIN CONCURRENCY CONTROL?

Concurrency control

Oracles multiversion concurrency control differs from the concurrency mechanism used by some other data base vendors. Read only queries are given a read –consistent snapshot which is view if the data base as it existed at the specific point in time, containing all update that we were committed by that point in time and not containing any updates that were not committed at any point in time thus read clock are not used in read only queries don't interfere with other data base activity in term of locking.

Managed stand by data base

To ensure high availability oracle provide a managed stand by data base
future A stand by data base is a copy of the regular data base ie in solved on the separate system. If a catastrophic failure occur on the primary system, the stand by system is activate and take over there by minimizing effect on failure on a availability. Oracle keeps the stand by data base up to date by constantly applying archived redo logs that are shipped from the primary data base the back up data base can be brought online in readonly mode and used for reporting and decision support queries

UNIT 5

1. WRITE SHORT NOTES ON DATA WARE HOUSING?

Data ware housing applications requires the transformation of data from many sources into a cohesive consistent step set of data configured appropriately for use in data ware house operation.

- **Distributed Transformation services**

  Data ware housing is an approach to manage data in which heterogeneous data sources are migrated to a separate homogeneous data base

- **Online Analytical processing services**

  OLAP services provide server and client capabilities to create and manage multidimensional OLAP data .

2. EXPLAIN NESTED RELATIONS?

Nested relations

The assumption of INF is a natural one in the bank examples wehave considered. However, not all applications are best modeled by INF relations.

The nested relational model is an extension of the relational model in which domains may be either atomic or relation valued.

We illustrate nested relations by an example from a library. Suppose we store for each book the following in formations

Book title
Set of authors
Publishers
Set of keywords

We can see that if we define a relation for the preceding information, several

domains will be monatomic

- **Authors**
- **Keywords**
- **Publishers**

Complex types
Collection and large object types
Create table books(
…
Keyword-set **setoff(varchar(20))**
…
)
Structure types
Creation of values of complex types

3. WHAT IS INHERITANCE? DESCRIBE IT IN DETAIL?

Inheritance

Inheritance can be at the levels of types, or at the level of tables We first consider inheritance of types, then inheritance at the level of labels.

Type inheritance

Suppose that we have the following type definition for people

create type person
(name **varchar**(20)
address **varchar**(20))

Table inheritance

Create table people **of** person

The consistency requirements for sub tables are

1. Each tuple of the sub table can correspond to at most one tuple in each of its immediate sub tables.
2. SQL:1999 has an additional constraint that all the tuples corresponding to each other must be derived from one tuple .

Overlapping sub tables

4 WHAT ARE THE TYPES OF REFERENCE?EXPLAIN IT WITH SUITABLE EXAMPLES?

Object oriented language provided the ability to refer the object attribute of the type can be referred to the specified type. We can define the type dept with a field name and a field head which is reference to the type person and a table dept of the type dept as followed

Create type dept(
Name **varchar(20),**
Head **ref**(person)**scope** people
)
Create table dept **of** dept

The table definition must specify that the reverence is derived and must still specify a self referential attribute name. When interesting a tuple for dept we can then use

Insert into dept
Values('CS','john')

5. DESCRIBE QUERIES WITH COMPLEX TYPES?

The present extension of the SQL query language deal with the complex type
Let us start with the simple example:
Find the title and the name of the publisher of each book this query carries out the task:

Select title, publisher.name
From books

- **path expression**

The reference are dereference in 1999 by the –> simple

Select head-> name, head->address
From dept

An expression such as" head->name" is called the path expression.

- **Collection valued attributes**
- **Nesting and unnesting**

The transformation of the nested relation in to a form with fewer (or no) the relation –valued attribute value is called unnesting

The reverse process of transformation a INF relation into a nested relation is called nesting**.**

UNIVERSITY QUESTIONS
PART A

UNIT I

1. List any two advantages of database system.
2. Give the reasons why null values might be introduces into database.
3. Compare database systems with file systems.
4. Give the distinction between primary key, candidate key and super key.
5. List 5 responsibilities of the DB manager.

6. Give the limitations of ER model? How do you overcome this?
7. What is data dictionary? What are the informations stored in the data dictionary?
8. Distinguish between physical &logical data independence.
9. Define database schema.
10. What are the responsibilities of DBA?

UNIT II

11. Write a SQL statement to find the names and loan numbers of all customers who have a loan at Chennai branch.
12. What is multi valued dependency?
13. What is static SQL? How does it differ from dynamic SQL.?
14. What are the different types of integrity constraints used in designing a relational database?
15. Define query language.
16. Why it is necessary to decompose a relation?
17. Define the term tuple.
18. What is the difference between primary key and foreign key.
19. What is View ? How it is created?
20. In what way is an Embedded SQL different from SQL? Discuss.
21. What is functional dependencies?
22. What are the desirable properties of decomposition?
23. What is referential integrity?
24. Explain the simple example with loss less join decomposition.

UNIT III

25. Give the measures of the quality of a disk.
26. What are the two types of ordered indices?
27. Compare sequential access devices versus random access devices with an example.
28. What can be done to reduce the occurrences of bucket overflows in a hash file organization?
29. Give any 2 advantages of spares index over dense index.
30. Name the different types of joins supported in SQL.
31. How do you choose the best evaluation plan for query?

UNIT IV

32. List out the ACID properties.
33. What is shadow paging?
34. Give the ACID properties.
35. State the benefits of strict two phase locking.
36. What are the types of transparencies that a distributed database must support? Why?
37. What benefit is provided by strict two phase locking?
38. What is time stamp ordering scheme?
39. Define Transactions.

UNIT V

40. Compare DBMS versus object oriented DBMS
41. What is the need for complex data types?
42. What is data mining?
43. What is data warehousing?
44. Briefly write the overall process of data ware housing.
45. What is an active database.
46. Give a comparison of object oriented and object relational databases.
47. Which are the 2 models used for discovering rules from databases?
48. Give the general forms of rules to express knowledge.
49. Define object relational databases.
50. Mention few applications of data warehousing.

PART B

UNIT I

1. (i) Describe the system structure of a database system.
   (ii) List out the functions of a DBA.
2. (i) Illustrate the issues to be considered while developing an ER diagram.
   (ii) Consider the relational database
   employee(empname,street,city)
   works(empname,companyname,salary)
   company(companyname,city)
   manages(empname,management)
   Give an expression in the relational algebra for each request.
   1) Find the names of all employees who work for First Bank Corporation.
   2) Find the names, street addresses and cities of residence of all employees who work for First Bank Corporation and earn more than 200000 per annum.
   3) Find the names of all employees in this database who live in the same city as the company for which they work.
   4) Find the names of all employees who earn more than every employees of small Bank Corporation
3. (i) Explain the system structure of a database system with neat Block diagram.
   (i) Construct the ER diagram for hospital with a set of patients and a set of medical doctors. Associate with each patient a log of the various tests and examinations conducted.
   (ii) Discuss on various related algebra operations with suitable Example.
4. (i) Compare file system with database system.
   (ii) Explain the architecture of DBMS.
5 (i) What are the steps involved in designing a database applications? Explain with an application.

(ii).List the possible types of relations that may exist between two entities. How would you realize that into tables for a binary relation?

6. (i) What are data models and how are they grouped?
   (ii) Explain in detail any two data models with sample databases
7. (i) Explain the component modules of a DBMS and their interaction with the architecture.
   (ii) Construct an ER diagram to a model online book store.
8. (i) Explain the basic Relational Algebra operations with the symbol used and an example for each.
   (ii) Discuss about Tuple relational Calculus and Domain relational Calculus

UNIT II

1. (i) What is normalization? Explain the various normalization techniques with suitable example.
   (ii) Give the comparison between BCNF and 3 NF.
   (ii) Discuss the strengths and weaknesses of the trigger mechanism. Compare triggers with other integrity constraints supported by SQL.

2) (i) Discuss about triggers. How do triggers offer a powerful mechanism for dealing with the changes to a database with suitable example.
   (ii) What are nested queries? Explain with example.
3. (i) What is normalization? Give the various normal forms of relational schema and define a relation which is in BCNF and explain with suitable example.
   (ii) Compare BCNF versus 3NF.
4 (i). What are the relational algebra operations supported in SQL? Write the SQL statement for each operation.
   (ii). Justify the need for Normalization with example.
5.(i) What is normalization? Explain 1NF,2NF,3NFand BCNF with Example.
   (ii). What is FD? Explain the role of FD in the process of normalization.
6. (i) SQL language has several parts .What are they?
   (ii) How many clauses are there in the basic structure of an SQL.
7. (i) Discuss the various pitfalls in a relational database design using a sample database.
   (ii) Explain at least two of the desirable properties of decomposition.

8 (i) Write short notes on the following:
Data Manipulation Language (DML), Data Definition Language (DDL)
Transaction Control Statements (TCS),Data Control Language (DCL)
Data Administration Statements (DAS).

(ii) Consider the database given by the following schemes.

Customer (Cust_No, Sales_ Person_No ,City)
Sales_ Person(Sales_ Person_No ,Sales_ Person_Name,
Common_Prec,Year_of_Hire)

Give an expression in SQL for each of the following queries:
Display the list of all customers by Cust_No with the city in which each is located.
List the names of the sales persons who have accounts in Delhi.

9. (i)Consider the universal relation r(A,B,C,D,E,F,G,H,I,J) and the set of FD's. G=({A,B}→ {C}→ {B,D}→ {E,F}, {A,D}→ {G,H}, {A}→{I}, {H}→{J}) What is the key of R? Decompose R into 2NF, then 3NF relations.

(ii) Discuss hoe schema refinement through dependency analysis and Normalization can improve schemas obtained through ER

UNIT III

1 (i) Explain how the RAID system improves performance and reliability.
(ii) Describe the structure of B+ tree and list the characteristics of a B+ tree.

2 (i) Explain the steps involved in processing a query.
(ii) Give the algorithm for Hash join.

3. (i) Describe about RAID levels.
(ii) Explain why allocations of records to blocks affects database system performance significantly.

4. (i) Describe the structure of B^+ tree and give the algorithm for search in the B^+ tree with example.
(ii) Give the comparison between ordered indexing and hashing.

5.(i). Explain the security features provided in commercial query languages.
(ii).What are the steps involved in query processing? How do you estimate the cost of the query?

6.(i) Explain the different properties of indexes in detail.
(ii) Explain various hashing techniques.

7 (i) What are the merits and demerits of B+ tree index structure.
(ii) How update operations are performed on b+ tree.

8. (i) What are the different types of storage media?
(ii) Explain with a diagram, the block storage operations.

9 (i) Describe the different types of file organization? Explain using a sketch of each of them with their advantages and disadvantages.
(ii) Describe static hashing and dynamic hashing.

10. (i) Explain the index schemas used in database systems.
(ii) How does a DBMS represent a relational query evaluation plan?

UNIT IV

1.(i) Describe about testing of serializability.
(ii) Discuss on two phase locking protocol.
2.(i) Explain the deferred and immediate modification versions of the log based recovery scheme.
(ii) Write short notes on shadow paging.
3. (i) Explain the different forms of Serializability.
(ii)What are different types of schedules are acceptable for recoverability.
4. (i) Discuss on two-phase locking protocol and time stamp-based protocol.
(ii) Write short notes on Log-based recovery.
5. (i) Explain the properties of transactions. Ilustrate the states of transactions.
(ii). What is RAID ? List the different levels in RAID technology and Explain it.
6. (i). What is concurrency Control? How is it implemented in DBMS?
(ii) Explain various recovery techniques during transactions in detail.
7.(i) Explain Time stamp-Based Concurrency Control protocol and the modifications implemented in it.
(ii) Describe shadow paging recovery techniques.
8.(i) Describe Strict Two-phase Locking protocol.
(ii) Explain Log-based recovery technique

UNIT V

1 (i) Highlight the features of OODBMS.
(ii) Write short notes on distributed databases.
2. (i) Give the structure of XML data.
(ii) Explain the architecture of a typical data warehouse and describe the various components of a data warehouse.
3.(i) Discuss in detail about the object relational databases and its advantages.
(ii) Illustrate the issues to implement distributed databases.

4. (i) Give the basic structure of XML and its document schema.
(ii) What are the two important classes of data mining problems? Explain about rule discovery using those classes.
5. (i) What are the types of Knowledge discovered data mining? Explain with suitable example.
(ii) Explain the structure of XML with suitable example.
6 .(i) What is commercial database system? Discus in detail.
(ii) Write a detailed notes on data mining .
7. (i) Explain 2-phase commitment protocol and the behaviour of the

Protocol during lost messages and site failure.
(ii) Describe X path and X query with an example.
8 (i) Explain Data Mining and Data Warehousing.
(ii) Describe the anatomy of XML document.

UNIVERSITY QUESTION PAPER NOV/DEC 2006

DATABASE MANAGEMENT SYSTEM(CS2255)

PART A

1. Compare database systems with file systems.
2. Give the distinction between primary key, candidate key and super key.
3. Write a SQL statement to find the names and loan numbers of all customers who have a loan at Chennai branch.
4. What is multi valued dependency?
5. Give the measures of the quality of a disk.
6. What are the two types of ordered indices?
7. List out the ACID properties.
8. What is shadow paging?
9. Compare DBMS versus object oriented DBMS.
10. What is data warehousing?

PART B

11.(a) (i) Describe the system structure of a database system.

(ii) List out the functions of a DBA.

(Or)

(b) (i) Illustrate the issues to be considered while developing an ER diagram.

(ii) Consider the relational database

employee(empname,street,city)
works(empname,companyname,salary)
company(companyname,city)
manages(empname,management)

Give an expression in the relational algebra for each request.

1) Find the names of all employees who work for First Bank Corporation.
2) Find the names, street addresses and cities of residence of all employees who work for First Bank Corporation and earn more than 200000 per annum.
3) Find the names of all employees in this database who live in the same city as the company for which they work.
4) Find the names of all employees who earn more than every employees of small Bank Corporation

12.(a) (i) Discuss about triggers. How do triggers offer a powerful mechanism for dealing with the changes to a database with suitable example.

(ii) What are nested queries? Explain with example.

(Or)

(b) (i) What is normalization? Give the various normal forms of relational schema and define a relation which is in BCNF and explain with suitable example.

(ii) Compare BCNF versus 3NF.

13.(a) (i) Describe about RAID levels.

(ii) Explain why allocations of records to blocks affects database system performance significantly.

(Or)

(b) (i) Describe the structure of B^+ tree and give the algorithm for search in the B^+ tree with example.

(ii) Give the comparison between ordered indexing and hashing.

14.(a) (i) Explain the different forms of Serializability.

(ii)What are different types of schedules are acceptable for recoverability.

(Or)

(b) (i) Discuss on two-phase locking protocol and time stamp-based protocol.

(ii) Write short notes on Log-based recovery.

15.(a) (i) Discuss in detail about the object relational databases and its advantages.

(ii) Illustrate the issues to implement distributed databases.

(Or)

(b) (i) Give the basic structure of XML and its document schema.

(ii) What are the two important classes of data mining problems? Explain about rule discovery using those classes.

UNIVERSITY QUESTION PAPER NOV/DEC 2007

DATABASE MANAGEMENT SYSTEM(CS2255)

PART A

1. List any two advantages of database system.
2. Give the reasons why null values might be introduces into database.
3. What is static SQL? How does it differ from dynamic SQL.?
4. What are the different types of integrity constraints used in designing a relational database?
5. Compare sequential access devices versus random access devices with an example.
6. What can be done to reduce the occurrences of bucket overflows in a hash file organization?
7. Give the ACID properties.
8. State the benefits of strict two phase locking.
9. What is the need for complex data types?
10. What is data mining?

PART B

11.(a) (i) Explain the system structure of a database system with neat Block diagram.

(Or)

(b)(i) Construct the ER diagram for hospital with a set of patients and a set of medical doctors. Associate with each patient a log of the various tests and examinations conducted.

(ii) Discuss on various related algebra operators with suitable Example.

12.(a) (i) Consider the employee database , where the primary keys are Underlined.

employee(empname,street,city)
works(empname,companyname,salary)
company(companyname,city)
manages(empname,management)

Give an expression in the relational algebra for each request.

1) Find the names of all employees who work for First Bank Corporation.
2) Find the names, street addresses and cities of residence of all employees who work for First Bank Corporation and earn more than 200000 per annum.
3) Find the names of all employees in this database who live in the same city as the company for which they work.
4) Find the names of all employees who earn more than every employees of small Bank Corporation.

(ii) Discuss the strengths and weaknesses of the trigger mechanism. Compare triggers with other integrity constraints supported by SQL.

(Or)

(b) (i) What is normalization? Explain the various normalization techniques with suitable example.

(ii) Give the comparison between BCNF and 3 NF.

13.(a) (i) Explain how the RAID system improves performance and reliability.

(ii) Describe the structure of B+ tree and list the characteristics of a B+ tree.

(Or)

(b) (i) Explain the steps involved in processing a query.
(ii) Give the algorithm for Hash join.

14.(a)(i) Describe about testing of serializability.
(ii) Discuss on two phase locking protocol.

(Or)

(b)(i) Explain the deferred and immediate modification versions of the log based recovery scheme.
(ii) Write short notes on shadow paging.

15.(a) (i) Highlight the features of OODBMS.
(ii) Write short notes on distributed databases.

(Or)

(b) (i) Give the structure of XML data.
(ii) Explain the architecture of a typical data warehouse and describe the various components of a data warehouse.

UNIVERSITY QUESTION PAPER NOV/DEC 2008

DATABASE MANAGEMENT SYSTEM (CS2255)

PART A

1. What is Database Management System? Why do we need a DBMS?
2. What are three characteristics of a relational database system?
3. State the differences between Security and Integrity.
4. What is decomposition and how does it address redundancy?
5. What is a heap file? How are pages organized in a heap file?
6. How does B-tree differ from a B^+ - tree ? Why is a B^+ - tree usually preferred as an access structure to a data file?
7. Give the meaning of the expression ACID transaction.
8. When are two schedules conflict equivalent?
9. Define the terms fragmentation and replication, in terms of where data is stored.

10. What are structured data types? What are collection types ,in particular?

PART B

11.(a) (i) Explain the component modules of a DBMS and their interactions with the architecture.

(ii) Construct an ER diagram to a model online book store.

(Or)

(b) (i) Explain the basic Relational Algebra operations with the symbol Used and an example for each.

(ii) Discuss about Tuple relational Calculus and Domain relational Calculus

12.(a) (i) Write short notes on the following:
Data Manipulation Language (DML)
Data Definition Language (DDL)
Transaction Control Statements (TCS)
Data Control Language (DCL)
Data Administration Statements (DAS).

(ii) Consider the database given by the following schemes.
Customer (Cust_No, Sales_ Person_No ,City)
Sales_ Person(Sales_ Person_No ,Sales_ Person_Name, Common_Prec,Year_of_Hire)
Give an expression in SQL for each of the following queries:
Display the list of all customers by Cust_No with the city in which each is located.
List the names of the sales persons who have accounts in Delhi.

(Or)

(b) (i)Consider the universal relation r(A,B,C,D,E,F,G,H,I,J) and the set of FD's. G=({A,B}→ {C}→ {B,D}→ {E,F}, {A,D}→ {G,H}, {A}→{I}, {H}→{J}) What is the key of R? Decompose R into 2NF,

then 3NF relations.

(ii) Discuss hoe schema refinement through dependency analysis and Normalization can improve schemas obtained through ER design.

13.(a) (i) Describe the different types of file organization? Explain using a sketch of each of them with their advantages and disadvantages.

(ii) Describe static hashing and dynamic hashing.

(Or)

(b) (i) Explain the index schemas used in database systems.

(ii) How does a DBMS represent a relational query evaluation plan?

14.(a) (i) Explain Time stamp-Based Concurrency Control protocol and the Modifications implemented in it.

(ii) Describe shadow paging recovery techniques.

(Or)

(b) (i) Describe Strict Two-phase Locking protocol.

(ii) Explain Log-based recovery technique.

15.(a) (i) Explain 2-phase commitment protocol and the behaviour of the Protocol during lost messages and site failure.

(ii) Describe X path and X query with an example.

(Or)

(b) (i) Explain Data Mining and Data Warehousing.

(ii) Describe the anatomy of XML document.

CS 2252 MICROPROCESSORS AND MICROCONTROLLERS

(Common to CSE & IT)

SYLLABUS

1.THE 8085 AND 8086 MICROPROCESSORS 9

8085 Microprocessor architecture-Addressing modes- Instruction set-Programming the 8085

2.8086 SOFTWARE ASPECTS 9

Intel 8086 microprocessor - Architecture - Signals- Instruction Set-Addressing Modes-Assembler Directives- Assembly Language Programming-Procedures-Macros-Interrupts And Interrupt Service Routines-BIOS function calls.

3. MULTIPROCESSOR CONFIGURATIONS 9

Coprocessor Configuration – Closely Coupled Configuration – Loosely Coupled Configuration – 8087 Numeric Data Processor – Data Types – Architecture –8089 I/O Processor –Architecture – Communication between CPU and IOP.

4. I/O INTERFACING 9

Memory interfacing and I/O interfacing with 8085 – parallel communication interface – serial communication interface – timer-keyboard/display controller – interrupt controller – DMA controller (8237) – applications – stepper motor – temperature control.

5. MICROCONTROLLERS 9

Architecture of 8051 Microcontroller – signals – I/O ports – memory – counters and timers – serial data I/O – interrupts-
Interfacing -keyboard, LCD,ADC & DAC

TOTAL: 45

TEXT BOOKS:

1. Ramesh S. Gaonkar ,"Microprocessor – Architecture, Programming and Applications with the 8085" Penram International Publisher , 5th Ed.,2006
2. Yn-cheng Liu,Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family architecture, Programming and Design", second edition, Prentice Hall of India , 2006 .
3. Kenneth J.Ayala, 'The 8051 microcontroller Architecture, Programming and applications' second edition ,Penram international.

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1. Douglas V.Hall, " Microprocessors and Interfacing : Programming and Hardware", second edition , Tata Mc Graw Hill ,2006.
2. A.K.Ray & K.M Bhurchandi, "Advanced Microprocessor and Peripherals – Architecture, Programming and Interfacing", Tata Mc Graw Hill , 2006.
3. Peter Abel, " IBM PC Assembly language and programming" , fifth edition, Pearson education / Prentice Hall of India Pvt.Ltd,2007.
4. Mohamed Ali Mazidi,Janice Gillispie Mazidi," The 8051 microcontroller and embedded systems using Assembly and C",second edition, Pearson education /Prentice hall of India , 2007.

UNIT I :THE 8085 AND 8086 MICROPROCESSORS

PART A

1. What is Microprocessor? Give the power supply & clock frequency of 8085.

A microprocessor is a multipurpose, programmable logic device that reads binary instructions from a storage device called memory accepts binary data as input and processes data according to those instructions and provides result as output. The power supply of 8085 is +5V and clock frequency in 3MHz.

2. List few applications of microprocessor-based system.

It is used:

i. For measurements, display and control of current, voltage, temperature, pressure, etc.

ii. For traffic control and industrial tool control.

iii. For speed control of machines.

3. What are the functions of an accumulator?

The accumulator is the register associated with the ALU operations and sometimes I/O operations. It is an integral part of ALU. It holds one of data to be processed by ALU. It also temporarily stores the result of the operation performed by the ALU.

4. List the 16 – bit registers of 8085 microprocessor.

Stack pointer (SP) and Program counter (PC).

5. List the allowed register pairs of 8085.

- B-C register pair
- D-E register pair
- H-L register pair

6. Mention the purpose of SID and SOD lines

SID (Serial input data line):

It is an input line through which the microprocessor accepts serial data.

SOD (Serial output data line):

It is an output line through which the microprocessor sends output serial data.

7. What is an Opcode?

The part of the instruction that specifies the operation to be performed is called the operation code or opcode

8. What is an Operand?

The data on which the operation is to be performed is called as an Operand

9. What is the function of IO/M signal in the 8085?

It is a status signal. It is used to differentiate between memory locations and I/O operations. When this signal is low (IO/M = 0) it denotes the memory related operations. When this signal is high (IO/M = 1) it denotes an I/O operation.

10. How many operations are there in the instruction set of 8085 microprocessor?

There are 74 operations in the 8085 microprocessor.

11. List out the five categories of the 8085 instructions. Give examples of the instructions for each group.

1. Data transfer group – MOV, MVI, LXI.
2. Arithmetic group – ADD, SUB, INR.
3. Logical group –ANA, XRA, CMP.
4. Branch group – JMP, JNZ, CALL.
5. Stack I/O and Machine control group – PUSH, POP, IN, HLT.

12. Explain the difference between a JMP instruction and CALL instruction.

A JMP instruction permanently changes the program counter. A CALL instruction leaves information on the stack so that the original program execution sequence can be resumed.

13. Explain the purpose of the I/O instructions IN and OUT.

The IN instruction is used to move data from an I/O port into the accumulator.

The OUT instruction is used to move data from the accumulator to an I/O port.

The IN & OUT instructions are used only on microprocessor, which use a separate address space for interfacing.

14. What is the difference between the shift and rotate instructions?

A rotate instruction is a closed loop instruction. That is, the data moved out at one end is put back in at the other end. The shift instruction loses the data that is moved out of the last bit locations.

15.Control signals used for DMA operation are _____

HOLD & HLDA.

16. What is meant by Wait State?

This state is used by slow peripheral devices. The peripheral devices can transfer the data to or from the microprocessor by using READY input line. The microprocessor remains in wait state as long as READY line is low. During the wait state, the contents of the address, address/data and control buses are held constant.

17. List the four instructions which control the interrupt structure of the 8085 microprocessor.

- DI (Disable Interrupts)
- EI (Enable Interrupts)
- RIM (Read Interrupt Masks)
- SIM (Set Interrupt Masks)

18. What is meant by polling?

Polling or device polling is a process which identifies the device that has interrupted the microprocessor.

19. What is meant by interrupt?

Interrupt is an external signal that causes a microprocessor to jump to a specific subroutine.

20. Explain priority interrupts of 8085.

The 8085 microprocessor has five interrupt inputs. They are TRAP, RST

7.5, RST 6.5, RST 5.5, and INTR. These interrupts have a fixed priority of interrupt service.

If two or more interrupts go high at the same time, the 8085 will service them on priority basis. The TRAP has the highest priority followed bye RST 7.5, RST 6.5, RST 5.5. The priority of interrupts in 8085 is shown in the table.

Interrupts Priority
TRAP
RST 7.5
RST 6.5
RST 5.5
INTR

21. What is a microcomputer?

A computer that is designed using a microprocessor as its CPU is called microcomputer.

22. What is the signal classification of 8085

All the signals of 8085 can be classified into 6 groups

- Address bus
- Data bus
- Control and status signals
- Power supply and frequency signals
- Externally initiated signals
- Serial I/O ports

23. What are operations performed on data in 8085

The various operations performed are

- Store 8-bit data
- Perform arithmetic and logical operations
- Test for conditions
- Sequence the execution of instructions
- Store data temporarily during execution in the defined R/W memory locations called the stack

24. Steps involved to fetch a byte in 8085

- The PC places the 16-bit memory address on the address bus
- . The control unit sends the control signal RD to enable the memory chip
- . The byte from the memory location is placed on the data bus
- . The byte is placed in the instruction decoder of the microprocessor and the task is carried out according to the instruction

25. How many interrupts does 8085 have, mention them

The 8085 has 5 interrupt signals; they are INTR, RST7.5, RST6.5, RST5.5 and TRAP

26. Basic concepts in memory interfacing

The primary function of memory interfacing is that the microprocessor should be able to read from and write into a given register of a memory chip. To perform these operations the microprocessor should

- Be able to select the chip
- Identify the register
- Enable the appropriate buffer

27. Define instruction cycle, machine cycle and T-state

Instruction cycle is defined, as the time required completing the execution of an instruction. Machine cycle is defined as the time required completing one operation of accessing memory, I/O or acknowledging an external request. T cycle is defined as one subdivision of the operation performed in one clock period

28. What is the use of ALE

The ALE is used to latch the lower order address so that it can be available in T2 and T3 and used for identifying the memory address. During T1 the ALE goes high, the latch is transparent ie, the output changes according to the input data, so the output of the latch is the lower order address. When ALE goes low the lower order address is latched until the next ALE.

29. How many machine cycles does 8085 have, mention them

The 8085 have seven machine cycles. They are

- Opcode fetch
- Memory read
- Memory write
- I/O read
- I/O write
- Interrupt acknowledge
- Bus idle

30. Explain the signals HOLD, READY and SID

HOLD indicates that a peripheral such as DMA controller is requesting the use of address bus, data bus and control bus. READY is used to delay the microprocessor read or write cycles until a slow responding peripheral is ready to send or accept data. SID is used to accept serial data bit by bit

31. Mention the categories of instruction and give two examples for each category

The instructions of 8085 can be categorized into the following five

- Data transfer MOV Rd,Rs STA 16-bit
- Arithmetic ADD R, DCR M
- Logical XRI 8-bit RAR
- Branching JNZ CALL 16-bit
- Machine control HLT NOP

32. Explain LDA, STA and DAA instructions

LDA copies the data byte into accumulator from the memory location specified by the 16-bit address. STA copies the data byte from the accumulator in the memory location specified by 16-bit address. DAA changes the contents of the accumulator from binary to 4-bit BCD digits.

33 Explain the different instruction formats with examples

The instruction set is grouped into the following formats

- One byte instruction MOV C,A
- Two byte instruction MVI A,39H
- Three byte instruction JMP 2345H

34. What is the use of addressing modes, mention the different types

The various formats of specifying the operands are called addressing modes, it is used to access the operands or data. The different types are as follows

- . Immediate addressing
- . Register addressing
- . Direct addressing
- . Indirect addressing
- . Implicit addressing

35. Why do we use XRA A instruction

The XRA A instruction is used to clear the contents of the Accumulator and store the value 00H.

36. Compare CALL and PUSH instructions

CALL PUSH

When CALL is executed the microprocessor automatically stores the 16-bit address of the instruction next to CALL on the stack. The programmer uses the instruction PUSH to save the contents of the register pair on the stack

When CALL is executed the stack pointer is decremented by two

When PUSH is executed the stack pointer register is decremented by two

PART B

1. **Explain the Architecture of 8085**.
   - ALU
   - Timing and control unit
   - Instruction Register & Decoding
   - Interrupt control
   - Serial I/O control

Ref diagram page no 59 Gaonkar

2..**Explain instruction sets of8085**.

- . Data transfer group – MOV, MVI, LXI.
- Arithmetic group – ADD, SUB, INR.
- Logical group –ANA, XRA, CMP.
- Branch group – JMP, JNZ, CALL.
- Stack I/O and Machine control group – PUSH, POP, IN, HLT.

3.**Explain Interrupts of 8085**.

- Maskable interrupt
- Non maskable interrupt
- Vectored interrupt
- Hardware interrupt
- Software interrupt

4**.Explain signal description of 8085**

- Address bus
- Control and status signal
- Address latch enable

- Read ,write signal
- S1,S0 status signals
- Power supply and clock frequency
- Externally initiated signals ,Including interrupts
- Serial I/O ports

5.**Explain addressing modes of 8085.**

- . Immediate addressing
- . Register addressing
- . Direct addressing
- . Indirect addressing
- Implicit addressing

UNIT-II 8086 SOFTWARE ASPECTS

PART A

1.What is the purpose of segment registers in 8086?

There are 4 segment registers present in 8086. They are

1. Code Segment (**CS**) register
2. Data Segment (**DS)** register
3. Stack Segment (**SS**) register
4. Extra Segment (**ES**) register

The **code segment** register gives the address of the current code segment. ie.It will points out where the instructions, to be executed, are stored in the memory.

The **data segment** register points out where the operands are stored in the memory.

The **stack segment** registers points out the address of the current stack, which is used to store the temporary results.

f the amount of data used is more the **Extra segment** register points out where the large amount of data is stored in the memory.

2. Define pipelining?

In 8086, to speedup the execution of program, the instructions fetching and execution of instructions are overlapped each other. This technique is known as pipelining.

In pipelining, when the n th instruction is executed, the n+1 th instruction is fetched and thus the processing speed is increased.

3. Discuss the function of instruction queue in 8086?

In 8086, a 6-byte instruction queue is presented at the Bus Interface Unit (BIU). It is used to pre fetch and store at the maximum of 6 bytes of instruction code from the memory. Due to this, overlapping instruction fetch with instruction execution increases the processing speed.

4. What is the maximum memory size that can be addressed by 8086?

In 8086, an memory location is addressed by 20 bit address and the address bus is 20 bit address and the address bus is 20 bits. So it can address up to one mega byte (2^20) of memory space.

5. What is the function of the signal in 8086?

BHE signal means Bus High Enable signal. The BHE signal is made low when there is some read or write operation is carried out. ie . When ever the data bus of the system is busy i.e. whenever there is some data transfer then the BHE signal is made low.

6.What are the predefined interrupts in 8086?

The various predefined interrupts are,

- DIVISION BY ZERO (type 0) Interrupt.
- SINGLE STEP (type 1) Interrupt.
- NONMASKABLE (type2) Interrupt.
- BREAK POINT (type 3) Interrupt.
- OVER FLOW (type 4) Interrupt.

7. What are the different flag available in status register of 8086?

There are 6 one bit flags are present. They are,

- AF - Auxiliary Carry Flag
- CF - Carry Flag
- OF - Overflow Flag
- SF - Sign Flag
- PF - Parity Flag
- ZF - Zero Flag

8. List the various addressing modes present in 8086?

There are 12 addressing modes present in 8086. They are,

(a) Register and immediate addressing modes

_ Register addressing modes

_ Immediate addressing mode

(b) Memory addressing modes.

Direct addressing modes

Register indirect addressing modes

Based addressing modes

Indexed addressing modes

Based Indexed addressing modes

String addressing modes

(c) I/O addressing modes

Direct addressing mode

Indirect addressing mode

(d) Relative addressing mode

(e) Implied addressing mode

9. How single stepping can be done in 8086?

By setting the Trace Flag (TF) the 8086 goes to single-step mode. In this mode, after the execution of each instruction s 8086 generates an internal interrupt and by writing some interrupt service routine we can display the content of desired registers and memory locations. So it is useful for debugging the program.

10. State the significance of LOCK signal in 8086?

If 8086 is working at maximum mode, there are multiprocessors are present. If the system bus is given to a processor then the LOCK signal is made low. That means the system bus is busy and it cannot be given of any other processors. After the use of the system bus again the LOCK signal is made high.

That means it is ready to give the system bus to any processor.

11. What are the functions of bus interface unit (BIU) in 8086?

(a) Fetch instructions from memory.
(b) Fetch data from memory and I/O ports.
(c) Write data to memory and I/O ports.
(d) To communicate with outside world.
(e) Provide external bus operations and bus control signals.

12. What is the clock frequency of 8086?

Internal clock Frequency 5 MHz 8MHz
External Clock Frequency 15MHZ 24MHZ

13. What are the two modes of operations present in 8086?

i. Minimum mode (or) Uniprocessor system
ii. Maximum mode (or) Multiprocessor system

14. Explain the process control instructions

STC – It sets the carry flag & does not affect any other flag
CLC – it resets the carry flag to zero &does not affect any other flag
CMC – It complements the carry flag & does not affect any other flag
STD – It sets the direction flag to 1 so that SI and/or DI can be decremented automatically after execution of string instruction & does not affect other flags
CLD – It resets the direction flag to 0 so that SI and/or DI can be incremented automatically after execution of string instruction & does not affect other flags
STI – Sets the interrupt flag to 1. Enables INTR of 8086.
CLI – Resets the interrupt flagto0. 8086 will not respond to INTR.

15. Compare Procedure & Macro

Accessed by CALL & RET instruction Accessed during assembly with name given during program execution to macro when defined Machine code for instruction is put only once in the memory Machine code is generated for instruction each time when macro is called With procedures less memory is required With macro more memory is required Parameters can be passed in registers, memory locations or stack
Parameters passed as part of statement which calls macro.

16. Define BIOS

The IBM PC has in its ROM a collection of routines, each of which performs some specific function such as reading a character from keyboard, writing character to CRT. This collection of routines is referred to as Basic Input Output System or BIOS.

17. Explain PUBLIC

For large programs several small modules are linked together. In order that the modules link together correctly any variable name or label referred to in other modules must be declared public in the module where it is defined. The PUBLIC directive is used to tell the assembler that a specified name or label will be accessed from other modules.
Format PUBLIC Symbol.

18. What are the 8086 interrupt types?

Dedicated interrupts

- Type 0: Divide by zero interrupt
- Type 1: Single step interrupt
- Type 2:Non maskable interrupt
- Type 3: Breakpoint
- Type 4: Overflow interrupt

Software interrupts

19. What is interrupt service routine?

Interrupt means to break the sequence of operation. While the CPU is executing a program an interrupt breaks the normal sequence of execution of instructions & diverts its execution to some other program. This program to which the control is transferred is called the interrupt service routine.

20. What are Macros?

Macro is a group of instruction. The macro assembler generates the code in the program each time where the macro is called. Macros are defined by MACRO & ENDM directives. Creating macro is similar to creating new opcodes that can be used in the program

```
INIT MACRO
MOV AX, data
MOV DS
MOV ES, AX
ENDM
```

21. What are procedures?

Procedures are a group of instructions stored as a separate program in memory and it is called from the main program whenever required. The type of procedure depends on where the procedures are stored in memory. If it is in the same code segment as that of the main program then it is a near procedure otherwise it is a far procedure.

22. What are the functions of status pins in 8086?

S2 S1 S0
0 0 0 ---- Interrupt acknowledge
0 0 1 ---- Read I/O
0 1 0 ---- Write I/O
0 1 1 ---- Halt
1 0 0 ---- Code access
1 0 1 ---- Read memory
1 1 0 ---- Write memory
1 1 1 ---- inactive
S4 S3
0 0 --I/O from extra segment
0 1 --I/O from Stack Segment
1 0 --I/O from Code segment
1 1 --I/O from Data segment
S5 --Status of interrupt enable flag
S6 --Hold acknowledge for system bus
S7 --Address transfer

PART-B

1. **Explain the signal description of 8086**.
   - Common signals
   - Bus high enable signals/Status

- Ready,INTR,TEST,NMI,RESET,CLK,
- Minimum mode signals
- maximum mode signals

Ref diagram page no 9 A.K.Ray

2. Explain the Architecture of 8086

i. special purpose registers
ii. General data register
iii. Segment registers
iv. Pointers and index registers
v. Bus interface unit
vi. Execution unit
vii. memory segmentation

Ref diagram page no 4 A.K.Ray

3..**Explain instruction sets of 8086.**

- Data transfer group – MOV,
- .Arithmetic group – ADD, SUB, INR.
- Logical group –AND, XOR, .
  Branch group – JP, JZ, CALL.
  Stack I/O and Machine control group – PUSH, POP, , HLT
- Processor control-CLC,CMC,STC,CLD
- String Manipulations.-MOVS,CMPS,SCAS

4. **. List the various addressing modes present in 8086?**

There are 12 addressing modes present in 8086. They are,
(a) Register and immediate addressing modes
Register addressing modes
_ Immediate addressing mode
(b) Memory addressing modes.
Direct addressing modes
Register indirect addressing modes
Based addressing modes
Indexed addressing modes
Based Indexed addressing modes
String addressing modes
(c) I/O addressing modes
Direct addressing mode
Indirect addressing mode
(d) Relative addressing mode
(e) Implied addressing mode

5**.Explain assembler Directives of 8086**

- DB,DW,DQ,DT
- END,ENDP,ENDS,EVEN,EQU,EXTRN
- GROUP,LABEL,LENGTH,LOCAL
- OFFSET,ORG,PROCEDURE
  PUBLIC,SEGMENT,SHORT,TYPE,GLOBAL

UNITIII: MULTIPROCESSOR CONFIGURATIONS

PART A

1. What are tightly coupled systems or closely coupled systems?

In a tightly coupled systems the microprocessor (either coprocessor or independent processors)may share a common clock and bus control logic.. The two processors in a closely coupled system may communicate using a common system bus or common memory.

2. What are loosely coupled systems?

In loosely coupled systems each CPU may have its own bus control logic. The bus arbitration is handled by an external circuit, common to all processors.. The loosely coupled system configuration like LAN & WAN can be spreaded over a large area.

3. Write some advantages of loosely coupled systems over tightly coupled systems

More number of CPUs can be added in a loosely coupled systems to improve the system performance.. The system structure is modular and hence easy to maintain and troubleshoot.

A fault in a single module does not lead to a complete system breakdown.

Due to the independent processing modules used in the system, it is more fault tolerant.

more suitable to parallel applications due to its modular organizations.

4. Write some disadvantages of loosely coupled systems

More complicated due to the required additional communication hardware.

They are less portable and more expensive due to the additional hardware and the communication media requirement.

5.Name some general purpose registers available in 8089processor.

Registers GA,GB,GC,BC,IX,MC

5. What is meant by Daisy Chaining method?

It does not require any priority resolving network, rather the priorities of all the devices are essentially assumed to be in sequence.

All the masters use a single bus request line for requesting the bus access. The controller sends a bus grant signal ,in response to the request ,if the busy signal is inactive when the bus is free. .The bus grant pulse goes to each of the masters in the sequence till it reaches a requesting master .The master then receives the grant signal, activates the busy line and gains the control of the bus. The priority is decided by the position of the requesting master in the sequence.

6. What is independent bus request scheme?

Each of the masters requires a pair of request and grant pins which are connected to the controlling logic. The busy line is common for all the masters. . f the controlling logic receives a request on a bus request line, it immediately grants the bus access using the corresponding bus grant signal, provided the BUSY line is inactive, and then grants the request.

This is quite fast ,because each of the masters can independently communicate with the controller.

7. What is meant by polling?

In polling schemes ,a set of address lines is driven by the controller to address each of the masters in sequence. When a bus request is received from a device by the controller, it generates the address on the address lines. .If the generated address matches with that of the requesting masters, the controller activates the BUSY line..
Once the busy line is activat3Write some advantages of loosely coupled systems ed ,the controller stops generating further address.

8. **Explain numeric processor 8087**.

Numeric processor 8087 is a coprocessor which has been designed to work under the control of the processor 8086 and offer it additional numeric processing capabilities.
What are CU and NEU in 8087?
CU-Control unit

NEU- Numeric extension unit. The numeric extension unit executes all the numeric processor instructions while the control unit receives ,decodes instructions ,reads and writes memory operands and executes 8087 control instructions. .These two units may work asynchronously with each other.

PART-B

1. **Explain the architecture of 8087**
   - control unit
   - Numeric extension unit
   - Register set of 8087

   Ref diagram page no 372 A.K.Ray

2. **Explain the Signal description of 8087**

   Ref diagram page no 373 A.K.Ray

3. **Explain the architecture of 8089**
   - Architecture diagram
   - Bus arbitration and control
   - Daisy chaining
   - Independent request
   - polling

   Ref diagram page no 393 A.K.Ray

UNIT IV: I/O INTERFACING

PART-A

1.What are the different types of methods used for data transmission?

The data transmission between two points involves unidirectional or bi-directional transmission of meaningful digital data through a medium. There are basically there modes of data transmission

(a) Simplex

(b) Duplex

(c) Half Duplex

In simplex mode, data is transmitted only in one direction over a single communication channel. For example, a computer (CPU is received by the computer (i.e the computer is receiver). However, it is not possible to transmit data from the computer to terminal and from terminal to the computer simultaneously.

2.What are the various programmed data transfer methods?

ii) Synchronous data transfer

iii) Asynchronous data transfer

iv) Interrupt driven data transfer

3. What is synchronous data transfer?

It is a data method which is used when the I/O device and the microprocessor match in speed. To transfer a data to or from the device, the user program issues a suitable instruction addressing the device. The data transfer is completed at the end of the execution of this instruction.

4. What is asynchronous data transfer?

It is a data transfer method which is used when the speed of an I/O device does not match with the speed of the microprocessor. Asynchronous data transfer is also called as Handshaking.

5. What are the functional types used in control words of 8251a?

The control words of 8251A are divided into two functional types.

1. Mode Instruction control word

2. Command Instruction control word

Mode Instruction control word :-This defines the general operational characteristics of 8251A.

Command Instruction control word:-The command instruction controls the actual operations of the selected format like enable transmit/receive, error reset and modem control.

6. What are the basic modes of operation of 8255?

There are two basic modes of operation of 8255, viz.

1. I/O mode.

3. BSR mode.

In I/O mode, the 8255 ports work as programmable I/O ports, while

In BSR mode only port C (PC0-PC7) can be used to set or reset its individual port bits. Under the IO mode of operation, further there are three modes of operation of 8 255, So as to support different types of applications, viz. mode 0, mode 1 and mode 2.

Mode 0 - Basic I/O mode

Mode 1 - Strobed I/O mode

Mode 2 - Strobed bi-directional I/O

7. Write the features of mode 0 in 8255?

1. Two 8-bit ports (port A and port B) and two 4-bit ports (port C upper and lower)

are available. The two 4-bit ports can be combined used as a third 8-bit port.

2. Any port can be used as an input or output port.

3.Output ports are latched. Input ports are not latched.

4. A maximum of four ports are available so that overall 16 I/O configurations are possible.

8. What are the features used mode 1 in 8255?

Two groups – group A and group B are available for strobed data transfer.

1. Each group contains one 8-bit data I/O port and one 4-bit control/data port.

2. The 8-bit data port can be either used as input or output port. The inputs and outputs both are latched.

3. Out of 8-bit port C, PC0-PC2 is used to generate control signals for port B and PC3=PC5 are used to generate control signals for port A. The lines PC6, PC7 may be used as independent data lines.

9. What are the signals used in input control signal & output control signal?

Input control signal

STB (Strobe input)

IBF (Input buffer full)

INTR(Interrupt request)

Output control signal

OBF (Output buffer full)

ACK (Acknowledge input)

INTR(Interrupt request)

10. What are the features used mode 2 in 8255?

The single 8-bit port in-group A is available.

1. The 8-bit port is bi-directional and additionally a 5-bit control port is available.
2. Three I/O lines are available at port C, viz PC2-PC0.
3. Inputs and outputs are both latched.
4. The 5-bit control port C (PC3=PC7) is used for generating/accepting handshake signals for the 8-bit data transfer on port A.

11. What are the modes of operations used in 8253?

Each of the three counters of 8253 can be operated in one of the following six modes of operation.

1. Mode 0 (Interrupt on terminal count)
2. Mode 1 (Programmable monoshot)
3. Mode 2 (Rate generator)
4. Mode 3 (Square wave generator)
5. Mode 4 (Software triggered strobe)
6. Mode 5 (Hardware triggered strobe)

12. What are the different types of write operations used in 8253?

There are two types of write operations in 8253

(1) Writing a control word register

(2) Writing a count value into a count register

The control word register accepts data from the data buffer and initializes the counters, as required. The control word register contents are used for

(a) Initializing the operating modes (mode 0-mode4)

(b) Selection of counters (counter 0- counter 2)

(c) Choosing binary /BCD counters
(d) Loading of the counter registers.
The mode control register is a write only register and the CPU cannot read its contents.

13. Give the different types of command words used in 8259a?

The command words of 8259A are classified in two groups

1. Initialization command words (ICWs)
2. Operation command words (OCWs)

14. Give the operating modes of 8259a?

(a) Fully Nested Mode
(b) End of Interrupt (EOI)
(c) Automatic Rotation
(d) Automatic EOI Mode
(e) Specific Rotation
(f) Special Mask Mode
(g) Edge and level Triggered Mode
(h) Reading 8259 Status
(i) Poll command
(j) Special Fully Nested Mode
(k) Buffered mode
(l) Cascade mode

15. What is the output modes used in 8279?

8279 provides two output modes for selecting the display options.

1.Display Scan

In this mode, 8279 provides 8 or 16 character-multiplexed displays those can be organized as dual 4-bit or single 8-bit display units.

2.Display Entry

8279 allows options for data entry on the displays. The display data is entered for display from the right side or from the left side.

16. What are the modes used in keyboard modes?

1. Scanned Keyboard mode with 2 Key Lockout.
2. Scanned Keyboard with N-key Rollover.
3. Scanned Keyboard special Error Mode.
4. Sensor Matrix Mode.

17. What are the modes used in display modes?

1. Left Entry mode

In the left entry mode, the data is entered from the left side of the display unit..

2. Right Entry Mode

In the right entry mode, the first entry to be displayed is entered on the rightmost display.

18. What is the use of modem control unit in 8251?

The modem control unit handles the modem handshake signals to coordinate the communication between the modem and the USART.

19. Give the register organization of 8257?

The 8257 perform the DMA operation over four independent DMA channels. Each of t he four channels of 8257 has a pair of two 16-bit registers. DMA address register and terminal count register. Also, there are two common registers for all the channels; namely, mode set registers and status register. Thus there are a total of ten registers. The CPU selects one of these ten registers using address lines A0- A3.

20. What is the function of DMA address register?

Each DMA channel has one DMA address register. The function of this register is to store the address of the starting memory location, which will be accessed by the DMA channel. Thus the starting address of the memory block that will be accessed by the device is first loaded in the DMA address register of the channel. Naturally, the device that wants to transfer data over a DMA channel, will access the block of memory with the starting address stored in the DMA Address Register.

21. What is the use of terminal count register?

Each of the four DMA channels of 8257 has one terminal count register. This 16-bit register is used for ascertaining that the data transfer through a DMA channel ceases or stops after the required number of DMA cycles.

22. What is the function of mode set register in 8257?

The mode set register is used for programming the 8257 as per the requirements of the system. The function of the mode set register is to enable the DMA channels individually and also to set the various modes of operation.

23. Distinguish between the memories mapped I/O peripheral I/O?

SL: NO **Memory Mapped I/O Peripheral I/O Peripheral I/O**

Memory Mapped I/O	**I/O mapped I/O**
16-bit device address	8-bit device address
Data transfer between any general-purpose register and I/O port.	Data is transfer only between accumulator and I.O port
The memory map (64K) is shared between I/O device and system memory	The I/O map is independent of the memory map; 256 input device and 256 output device can be connected
More hardware is required to decode 16-bit address	Less hardware is required to decode 8-bit address
Arithmetic or logic operation can be directly performed with I/O data	Arithmetic or logical operation cannot be directly performed with I/O data

24. List the operation modes of 8255

a) I.O Mode

i. Mode 0-Simple Input/Output.

ii. Mode 1-Strobed Input/Output (Handshake mode)

iii. Mode 2-Strobed bidirectional mode
b) Bit Set/Reset Mode.

25. **What is a control word?**

It is a word stored in a register (control register) used to control the operation of a program digital device.

26. **What is the purpose of control word written to control register in 8255?**

The control words written to control register specify an I/O function for each I.O port. The bit D7 of the control word determines either the I/O function of the BSR function.

27.What is the size of ports in 8255?

Port-A : 8-bits
Port-B : 8-bits
Port-CU : 4-bits
Port-CL : 4-bits

28. What is interfacing?

An interface is a shared boundary between the devices which involves sharing information. Interfacing is the process of making two different systems communicate with each other.

29. What is memory mapping?

The assignment of memory addresses to various registers in a memory chip is called as memory mapping.

30. What is I/O mapping?

The assignment of addresses to various I/O devices in the memory chip is called as I/O mapping.

31. What is an USART?

USART stands for universal synchronous/Asynchronous Receiver/ Transmitter. It is a programmable communication interface that can communicate by using either synchronous or asynchronous serial data.

32.What is the use of 8251 chip?

8251 chip is mainly used as the asynchronous serial interface between the processor and the external equipment.

33. The 8279 is a programmable _____ interface.

Keyboard/Display

34. List the major components of the keyboard/Display interface.

a. Keyboard section
b. Scan section
c. Display section
d. CPU interface section

35. What is Key bouncing?

Mechanical switches are used as keys in most of the keyboards. When a key is pressed the contact bounce back and forth and settle down only after a small time delay (about 20ms). Even though a key is actuated once, it will appear to have been actuated several times. This problem is called Key Bouncing.

36.Define HRQ?

The hold request output requests the access of the system bus. In non- cascaded 8257 systems, this is connected with HOLD pin of CPU. In cascade

mode, this pin of a slave is connected with a DRQ input line of the master 8257, while that of the master is connected with HOLD input of the CPU.

37. What is the use of stepper motor?

A stepper motor is a device used to obtain an accurate position control of rotating shafts. A stepper motor employs rotation of its shaft in terms of steps, rather than continuous rotation as in case of AC or DC motor.

38. What is TXD?

TXD- Transmitter Data Output

This output pin carries serial stream of the transmitted data bits along with other information like start bit, stop bits and priority bit.

39. What is RXD?

RXD- Receive Data Input

This input pin of 8251A receives a composite stream of the data to be received by 8251A.

PART-B

1. **Explain Programmable Interrupt controller with neat diagram.**
   Features
   - Block diagram
   - Initialisation command word
   - Interrupt sequence
   - Interrupt Request Register
   - In service register
   - Priority Resolver
   - Interrupt mask register
   - Data bus buffer

   Ref diagram page no 226 A.K.Ray

2. **Explain 8253/8254 Timer**
   - Operation modes
   - Mode0-Interrupt on terminal count
   - Mode1-HW triggered /programmable one shot
   - Mode2-Rate generator
   - Mode3-Squre wave generator
   - Mode4-software triggered strobe
   - Mode5 -Hardware triggered strobe

   Ref diagram page no A.K.Ray

3. **Explain DMA controller 8237**
   - 8237 DMA controller
   - Signal description of 8237
   - Register organizations of 8257
   - DMA address registers
   - Terminal count registers

- Mode set registers
- Status registers
- Data bus buffer ,priority resolver

Ref diagram page no268 A.K.Ray

4. **8279 programmmable keyboard/Display interface**
   - Pin configuration
   - Block diagram of 8279
   - Keyboard section,scan section ,display section,MPU interface section
   - Programming 8279
   - Parallel communication interface
   - Pin configuration Architecture of 8255
   - control logic, control word

Ref diagram page no 240 A.K .Ray

5 .**Serial communication interface((8251 USART)**
   - Architecture of 8251
   - Operating modes
   - Asynchronous mode
     Synchronous mode

Ref diagram page no 252 A.K.Ray

UNIT V: MICROCONTROLLERS

PART-A

1. What is meant by microcontroller?

A device which contains the microprocessor with integrated peripherals like memory, serial ports, parallel ports, timer/counter, interrupt controller, data acquisition interfaces like ADC,DAC is called microcontroller.

2. Explain DJNZ instructions of intel 8051 microcontroller?

a) DJNZ Rn, rel

Decrement the content of the register Rn and jump if not zero.

b) DJNZ direct , rel

Decrement the content of direct 8-bit address and jump if not zero.

3. State the function of RS1 and RS0 bits in the flag register of intel 8051 microcontroller?

RS1 , RS0 – Register bank select bits

RS1	RS0	BankSelection
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

4. Give the alternate functions for the port pins of port3?

RD – Read data control output.

WR – Write data control output.

T1 – Timer / Counter1 external input or test pin.
T0 – Timer / Counter0 external input or test pin.
INT1- Interrupt 1 input pin.
INT 0 – Interrupt 0 input pin.
TXD – Transmit data pin for serial port in UART mode.
RXD - Receive data pin for serial port in UART mode

5. **Explain the function of the pins PSEN and EA of 8051**.

PSEN: PSEN stands for program store enable. In 8051 based system in which an external ROM holds the program code, this pin is connected to the OE pin of the ROM.

EA :EA stands for external access. When the EA pin is connected to Vcc, program fetched to addresses 0000H through 0FFFH are directed to the internal ROM and program fetches to addresses 1000H through FFFFH are directed to external ROM/EPROM. When the EA pin is grounded, all addresses fetched by program are directed to the external ROM/EPROM.

6. Explain the 16-bit registers DPTR and SP of 8051.

DPTR:

DPTR stands for data pointer. DPTR consists of a high byte (DPH) and a low byte (DPL). Its function is to hold a 16-bit address. It may be manipulated as a 16-bit data register or as two independent 8-bit registers. It serves as a base register in indirect jumps, lookup table instructions and external data transfer.

SP:

SP stands for stack pointer. SP is a 8- bit wide register. It is incremented before data is stored during PUSH and CALL instructions. The stack array can reside anywhere in on-chip RAM. The stack pointer is initialised to 07H after a reset. This causes the stack to begin at location
08H.

7. Name the special functions registers available in 8051.

- Accumulator
- B Register
- Program Status Word.
- Stack Pointer.
- Data Pointer.
- Port 0
- Port 1
- Port 2
- Port 3
- Interrupt priority control register.

8. Compare Microprocessor and Microcontroller.

Microprocessor	**Microcontroller**
Microprocessor contains ALU, general purpose registers, stack pointer, program counter, clock timing circuit and interrupt circuit.	Microcontroller contains the circuitry of microprocessor and in addition it has built- in ROM, RAM, I/O devices, timers and counters.

It has many instructions to move data between memory and CPU	It has one or two instructions to move data between memory and CPU.
It has one or two bit handling Instructions	It has many bit handling instructions.
4 Access times for memory and I/O devices are more.	Less access times for built-in memory and I/O devices
Microprocessor based system requires more hardware.	Microcontroller based system requires less hardware reducing PCB size and increasing the reliability.

9.Name the five interrupt sources of 8051?.

The interrupts are:

Vector address

- External interrupt 0 : IE0 : 0003H
- Timer interrupt 0 : TF0 : 000BH
- External interrupt 1 : IE1 : 0013H
- Timer Interrupt 1 : TF1 : 001BH
- Serial Interrupt

Receive interrupt : RI : 0023H

Transmit interrupt: TI : 0023H

- Interrupt enable control register.

PART-B

1.**Explain architecture of 8051**

- Accumulator, B regisrer, PSW, Stack pointer
- Data pointer,port0to 3 latches and drives, serial data buffer
- Timer, Registers,control register,Timing and control unit,oscillator,ALU,SFR Reg
- PSW,8051 registerbank,stack in 8051,TMOD,TCON,SCON,PCON

Ref diagram page no 604 A.K.Ray

-

2.**Explain instruction sets of 8051**

- . Data transfer group
- Arithmetic group
- . Logical group –.
- . Branch group –.
- . Stack I/O and Machine control group

3. **Applications of 8051**

- Stepper motor interfacing
- Length measurement
- Square wave generator

UNIVERSITY QUESTION PAPER

B.E/B.TECH DEGREE EXAMINATION NOV/DEC 2006

PART-A

1.Name the flag bits available in 8085 microprocessors.

The 8085 microprocessor has five flags to indicate five different types of data conditions .they are zero(Z),carry(CY),Sign (S),Parity(P) and auxillary carry(AC) flags.The most commonly used flags are sign ,zero and carry.

2.Give the significance of SIM and RIM instruction available in 8085.

Instruction SIM: Set Interrupt Mask. this is a 1 byte instruction and can be used three different functions as follows

i)to set mask for RST 7.5,6.5 AND 5.5 INTERRUPTS.

ii) to reset RST 7.5 Flip Flop.

iii)to implement serial I/O operation.

Instruction RIM: Read Interrupt Mask .this is a 1 byte instruction and can be used for the following three functions.

i)to read interrupt masks.

ii)to identify pending interrupts.

iii)to receive serial data.

3.What do you mean by pipelining in an 8086 processor?

The computer is composed of two parts that operate asynchronously one part called a BIU in the 8086,fetches instruction from code memory whenever the memory is free .another part called EU in the 8086 executes instructions on a continuous basis. the BIU gets instruction bytes and shifts them in an internal memory called instruction queue or pipe line.

4.How the 20 bit effective address is calculated in an 8086 processor?

5.What is the purpose of clock signal in an 8086 system?

8086 require clock signal with 33%duty cycle from some external operations.8086 processor requires 5 MHZ clock signal.

6.What is the use of latch signal on the AD0-AD15 bus in an 8086 system?

Latch signal is used to load the data those are fetched from memory to bus.

7.Name the three modes used by the DMA processor to transfer data?

Signal transfer mode(cycling stealing mode)

Block transfer mode

Demand transfer mode

8.Name the 6 modes of operations of an 8253 programmable interval timer.

Mode 0:interrupt on terminal count

Mode 1:hardware re -triggerable one-shot

Mode 2 :rate generator

Mode3:square wave rate generator

Mode 4:software triggered strobe

Mode 5:hardware triggered strobe

9.Differentiate a Microprocessor and a Microcontrollers

Microprocessor	Microcontroller
1.Chip on computer 2.8 bit data bus 8 bit address bus 3.It cant perform any task without external device. 4.No internal memory &interfacing devices.	1.It is a mini computer 2. 16 bit data bus 16bit address bus 3.It contains microprocessor to perform any task. 4.Internal memory &some interfacing devices within the chip.

10.Differentiate RRA and RRCA in 8051 microcontroller.

RRA	RRCA
1.Rotate Accumulator Right. 2.The 8 bits in accumulator are rotated one bit to right. 3.No flags are affected	1.Rotate Accumulator Right through carry flag. 2.The 8 bits in accumulator and carry flag are together rotated one bit to the right.bit 0 moves into the carry flag,the original value of carry flag moves to bit 7 position. 3.No flags are affected

PART B

11(a)Explain 8085 microprocessor with functional block diagram
Ref diagram page no 59 Microprocessor,Architecture,Programming and Applications RAMESH.S.GAONKAR

or

(b)Explain programming techniques of 8085.

12 (a) write about instruction set of 8086.
Ref page no 44&45 Advanced Microprocessors and Peripherals A.K RAY

or

(b)Describe the addressing mode of 8086
Ref page no 36 Advanced Microprocessors and Peripherals A.K RAY

14(a)Describe DMA controller 8257 internal architecture.
Ref diagram page no268 Advanced Microprocessors and Peripherals A.K RAY

or

14(b)Explain mode of operation and command words of 8279
Ref diagram page no 240 Advanced Microprocessors and Peripherals A.K RA

15(a)Explain the operations of 8051

Ref diagram page no 604 Advanced Microprocessors and Peripherals A.K RAY

or

(b)Describe interrupts and instruction set of 8051.

- Data transfer group
- Arithmetic group
- . Logical group –.
- . Branch group –.
- . Stack I/O and Machine control group

B.E/B.TECH DEGREE EXAMINATION MAY/JUNE 2007

MICROPROCESSOR AND MICROCONTROLLER

PART-A

1.How address and data lines are demultiplexed in 8085?

AD0-AD7 lines are multiplexed and the lower half of address A0-A7 is available only during T1 of the machine cycle. this lower half of address is also necessary during T2 and T3 of the machine cycle lower half of address is also necessary during T2 &T3 of machine cycle to access specific location in memory or I/O part .this means that the lower half of an address bus must be latched in T1 of the machine cycle. the latching of lower half of an address is done by using external latch and ALE signal from 8085.

2.what is the function performed by SIM instruction in 8085?

SIM –Set Interrupt Mask. This instruction masks the interrupts as desired .it also sends out serial data through the serial output data (SOD) pin .For this instruction command byte must be loaded in the accumulator.

3.what is pipelined architecture?

The computer is composed of two parts that operate asynchronously one part called a BIU, fetches instruction from code memory whenever the memory is free. another part called EU in the 8086 executes instruction on a continuous basis .the BIU gets instruction bytes and stuffs memory in an internal memory called instruction queue or pipeline.

4.how the interrupts can be masked/unmasked in 8086?

The 8086 interrupt priorities are concerned, software interrupts have the highest priority, followed by NMI followed by INTR. The lowest priority signals are un maskable interrupts.

5.what are the signals involved in memory bank selection in 8086 microprocessor?

The 8086 based system will have two sets of memory IC's.One set for even bank and another for odd bank. The data lines D0-D7 are connected to even bank and the data lines D8-D15 are connected to odd bank .the even memory bank is selected by address line A0and odd memory bank is selected by control signal BHE .The memory banks are selected ahen these signals are active low.

6.how clock signal is generated in 8086?what is the maximum internal clock frequency of 8086?

Clock input 33% square wave from external clock generator .the external clock generator is used to provide timing for all CPU function .the 8086 requires one phase clock with a 33%duty cycle to provide internal timing .the maximum internal frequency required by 8086 is 5 MHZ.

7.What is the function of gate signal in 8254 timer?

The 8254 has three independent 16-bit counters, which can be programmed to. work in any one of possible six modes .each counter has a clock input gate input and counter output .to operate a counter ,a count value has to be loaded in count register, gate should be tied high and a clock signal should be applied through clock input .the counter counts by decrementing the count value by one in each cycle of clock signal and generates output.

8.write the format of ICW1 in 8259?

9.list the interrupts of 8051 microcontroller.

External interrupts-INT0 &INT1

Timer interrupts-TF0&TF1

10.what are register banks banks in 8051 microcontroller?

RS1	RS0	BAND SELECTION
0	0	BANK 0
0	1	BANK 1
1	0	BANK 2
1	1	BANK 3

PARTB

11) A)(i) Explain the various logical and arithmetic instructions available in 8085 microprocessor.

Ref page no 48 Microprocessor,Architecture,Programming and Applications RAMESH.S.GAONKAR

ii) Explain the function of various flags of 8085 microprocessor.

Ref page no 141 Microprocessor,Architecture,Programming and Applications RAMESH.S.GAONKAR

Or

B()i) Differentiate I/O mapped I/O and memory mapped I/O

Ref page no 123 Microprocessor,Architecture,Programming and Applications RAMESH.S.GAONKAR

(ii) Write an 8085 assembly language program to convert an 8 bit binary to ASCII code.

12 (a).Describe the action taken by 8086 when INTR pin is activated.

Ref page no 44&45 Advanced Microprocessors and Peripherals A.K RAY

(ii) write an assembly language program in 8086 to search the largest data in an array.

Or

B (i) Discuss the various addressing modes of 8086 microprocessor

(ii) Explain the following assembler directives used in 8086

1)ASSUME

2)EQU

3)DW

13(a) Explain in detail about memory access mechanism in 8086

Ref page no 15& 613 Advanced Microprocessors and Peripherals A.K RAY

Or

(b)(i) Draw and explain a block diagram showing 8086 in maximum mode configuration

Ref page no 22 Advanced Microprocessors and Peripherals A.K RAY

(ii) What are the advantages of the multiprocessor systems?

Ref page no 363 Advanced Microprocessors and Peripherals A.K RAY

14(a) With the help of block diagram explain the operation of USART

Ref page no 256 Advanced Microprocessors and Peripherals A.K RAY

(ii) Discuss the salient features of 8259 programmable interrupt controller.

Ref page no 226 Advanced Microprocessors and Peripherals A.K RAY

Or

(b)(i)Describe the various modes of operation in 8253 programmable interval timer.

Ref page no 215 Advanced Microprocessors and Peripherals A.K RAY

(ii)Explain the operation of DMA controller(8237)

Ref page no 268 Advanced Microprocessors and Peripherals A.K RAY

15.(a) With suitable diagram the architecture of 8051 microcontroller.

Ref page no 54 The 8051 Microcontroller-KENNETH.J.AYALA

Or

(b) Discuss in detail about 8051 based stepper motor control along with necessary hardware and software.

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PART-A

1.List the different types of flags affected by the arithmetic and logic operations.

Carry flag, auxillary carry flag ,parity flag, sign flag, zero flag

2.Draw the contents of the stack and the regist ers after a push instruction.

3.What do these 8086 instructions do?

STD-Set Direction Flag. when the instruction is executed ,the direction flag of 8086 is set to 1.

IRET-Interrupt Return. this instruction is used to terminate an interrupt service procedure and transfer the program control back to main program.

4.What is macro?

A macro is a group of instructions written within brackets and identified by a name .this is used when a repeated group of instructions is too short or not appropriate to be written as a subroutine.

5.Draw a simple block diagram of a microprocessor based water-level indicator.

6.What is a coprocessor?

It is a specially designed microprocessor which take care of mathematical calculations involving integer and floating point data .it is designed to work in parallel with a processor.

7.List the uses of USART.

USART-Universal Synchronous Asynchronous Receiver-Transmitters.

It is used to transmit and receive the data in serial communication mode.

It is used to convert parallel data into serial data or vice-versa

It is used to interface MODEM and establish serial communication MODEM over telephone lines.

8.Calculate how many devices can be addressed by 8086.

9.Draw the format of PSW of 8051.

10.List the addressing modes supported by 8051.

1.Register addressing
2.Direct addressing
3.Register indirect addressing
4.Immediate addressing
5.Register addressing
6.Index addressing

PART B

11(a)(I) Draw the timing diagram for SHLD 16bit address

Ref page no 124 Microprocessor,Architecture,Programming and Applications RAMESH.S.GAONKAR

(ii)Write an 8085 ALP to convert hexadecimal value to decimal value.

Or

(ii) Draw and discuss the internal architecture of 8085 in detail

Ref page no 25 Microprocessor,Architecture,Programming and Applications RAMESH.S.GAONKAR

12(a)(i) Discuss in detail the data related addressing modes of 8086 with an example.

Ref page no 226 Advanced Microprocessors and Peripherals A.K RAY

(ii) Write an 8086 ALP to reverse a string

Or

b).Discuss in detail the interrupts and interrupt service routine

Ref page no 125 Advanced Microprocessors and Peripherals A.K RAY

14. a)Discuss how the DMA controller is interfaced with 8085 processor.

Ref page no 497 Microprocessor,Architecture,Programming and Applications RAMESH.S.GAONKAR

or

b) Discuss in detail about programmable interrupt controller and its cascading mode of operation.

Ref page no 488 Microprocessor,Architecture,Programming and Applications RAMESH.S.GAONKAR

15(a)Discuss the register set of 8051 and also discuss how memory and I/O addressing is done in 8051.

Ref page no 62 The 8051 Microcontroller-KENNETH.J.AYALA

or

b)Discuss in detail the internal architecture of an 8051 microcontroller.

Ref page no 54 The 8051 Microcontroller-KENNETH.J.AYALA

CS 2253 COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to CSE & IT)

SYLLABUS

1. Basic Structure of Computers 9

Functional units – Basic operational concepts – Bus structures – Performance and metrics – Instructions and instruction sequencing – Hardware – Software Interface – Instruction set architecture – Addressing modes – RISC – CISC. ALU design – Fixed point and floating point operations.

2. Basic Processing Unit 9

Fundamental concepts – Execution of a complete instruction – Multiple bus organization – Hardwired control – Micro programmed control – Nano programming.

3. Pipelining 9

Basic concepts – Data hazards – Instruction hazards – Influence on instruction sets – Data path and control considerations – Performance considerations – Exception handling.

4. Memory System 9

Basic concepts – Semiconductor RAM – ROM – Speed – Size and cost – Cache memories – Improving cache performance – Virtual memory – Memory management requirements – Associative memories – Secondary storage devices.

5. I/O Organization 9

Accessing I/O devices – Programmed Input/Output -Interrupts – Direct Memory Access – Buses – Interface circuits – Standard I/O Interfaces (PCI, SCSI, USB), I/O devices and processors.

Text Book:

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”, Fifth Edition, Tata McGraw Hill, 2002.

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1. David A. Patterson and John L. Hennessy, “Computer Organization and Design: The Hardware/Software interface”, Third Edition, Elsevier, 2005.
2. William Stallings, “Computer Organization and Architecture – Designing for Performance”, Sixth Edition, Pearson Education, 2003.
3. John P. Hayes, “Computer Architecture and Organization”, Third Edition, Tata McGraw Hill, 1998.
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PART – A QUESTIONS

UNIT-I

1 .What is cache memory?

The small and fast RAM units are called as caches. When the execution of an instruction calls for data located in main memory, the data are fetched and a copy is placed in the cache. Later if the same data is required it is read directly from the cache.

2. What is the function of ALU?

Most of the computer operations(arithmetic and logic)are performed in ALU. The data required for the operation is brought by the processor and the operation is performed by ALU.

3. What is the function of CU?

The control unit acts as the nerve center, that coordinates all the computer operations. It issues timing signals that governs the data transfer.

4. What are the basic operations of a computer?

The basic operations are READ and WRITE.

5. What are the registers generally contained in the processor?

MAR-memory address register
MDR-memory data register
IR-Instruction Register
RO-Rn-General purpose register
PC-Program counter

6. What are the steps in executing the program?

1.fetch
2.decode
3.execute
4.store

7. Define interrupt and ISR?

An interrupt is a request from an I/O device for service by the processor. The processor provides the requested service by executing the interrupt service routine.

8. Define bus?

A group of lines that serves as a connecting path for several devices is called a bus.

9. What is the use of buffer register?

The buffer register is used to avoid speed mismatch between the I/O device and the processor.

10. Compare single bus structure and multiple bus structure?

A system that contains only one bus(i.e only one transfer at a time) is called as a single bus structure. A system is called as multiple bus structure if it contains multiple buses.

11. What is system software? Give an example.

It is a collection of program that are executed as needed to perform functions such as

I. receiving and interpreting user commands
II. entering and editing application programs and storing them as files in secondary storage devices.

Eg. assembler, linker, compiler etc

12. What is application software? Give example.

Application programs are usually written in a high level programming language, in which the programmer specifies mathematical or text processing operations. These operations are described in a format that is independent of the particular computer used to execute the program.
Ex: C,C++,JAVA

13. What is compiler?

A system software program called a compiler translates the high-level language program into a suitable machine language program containing instruction such as the Add and Load instructions.

14. what is text editor?

It is used for entering and editing application programs. The user of this program interactively executes command that allow statements of a source program entered at a keyboard to be accumulated in a file.

15. Discuss about OS as system software?

OS is a large program or actually a collection of routines, that is used to control the sharing of and interaction among various computer units as they execute application programs. The OS routines perform the tasks required to assign computer resources to individual application programs.

16. What is multiprogramming or multitasking?

The operating system manages the concurrent execution of several application programs to make the best possible uses of computer resources. This pattern of concurrent execution is called multiprogramming or multitasking.

17. What is elapsed time of computer system?

The total time to execute the total program is called elapsed time. it is affected by the speed of the processor, the disk and the printer.

18. What is processor time of a program?

The periods during which the processor is active is called processor time of a program it depends on the hardware involved in the execution of individual machine instructions.

19. Define clock rate?

The clock rate is given by, R=1/P, where P is the length of one clock cycle.

20. Write down the basic performance equation?

T=N*S/R
T=processor time
N=no.of instructions
S=no of steps
R=clock rate

21. What is pipelining?

The overlapping of execution of successive instructions is called pipelining.

22. What is byte addressable memory?

The assignment of successive addresses to successive byte locations in the memory is called byte addressable memory.

23. What is big endian and little endian format?

The name big endian is used when lower byte addresses are used for the more significant of the word. The name little endian is used for the less significant bytes of the word.

24. What is branch instruction?

As a result of branch instruction is a type of instruction which loads a new values into the program counter.

25. What is branch target?

As a result of branch instruction, the processor fetches and executes the instruction at a new address called branch target, instead of the instruction at the location that follows the branch instruction in sequential address order.

26. What are condition code flags?

The processor keeps track of information about the results of various operations for use by subsequent conditional branch instructions. This is accomplished by recording the required information in individual bits, often called condition code flags.

27. Define addressing modes.

The different ways in which the location of an operand is specified in an instruction are referred to as addressing modes.

28. What is a pointer?

The register or memory location that contains the address of an operand is called a pointer.

29. What is index register?

In index mode the effective address of the operand is generated by adding a constant value to the contents of a register. The register used may be either a special register or may be any one of a set of general purpose register in the processor. This register is referred to as an index register.

30. What is assembly language?

A complete set of symbolic names and rules for the use of machines constitute a programming language, generally referred to as an assembly language.

31. What is assembler directive?

SUM EQU 200
Assembler directives are not instructions that will be executed. It simply informs the assembler that the name SUM should be replaced by the value 200 wherever it appears in the program, such statements are called as assembler directives.

32. What is loader?

Loader is a system software which contains a set of utility programs. It will load the object program to the memory.

33. Define device interface.

The buffer registers DATAIN and DATAOUT and the status flags SIN and SOUT are part of circuitry commonly known as a device interface.

34. Briefly explain the floating point representation with an example?

The floating point representation has 3 fields
1.sign bit
2.siginificant bits
3.exponent
For example consider 1.11101100110*10’5.
Mantissa=11101100110
Sign=0
Exponent =5

35. What are the 2 IEEE standards for floating point numbers?

1.single
2.double

36. What is overflow, underflow case in single precision(sp)?

Underflow-In SP it means that the normalized representation requires an exponent less than -126.
Overflow-In SP it means that the normalized representation requires an exponent greater than +127.

37. What are the exceptions encountered for FP operation?

The exceptions encountered for FP operation are overflow, underflow. /0, inexact and invalid values.

38. What is guard bits?

guard bits are extra bits which are produced during the intermediate steps to yield maximum accuracy in the final results.

39. What are the ways to truncate guard bits?

1.chopping
2.von Neumann rounding
3.rounding procedure.

UNIT II

1. Explain MDR and MAR.

The data and address lines of the external memory bus connected to the internal processor bus via the memory data register, MDR,and the memory address register , MAR, respectively. Register MDR has two inpits and two outputs. Data may be loaded into MDR either from the memory bus or from the internal processor bus the data stored in MDR may be placed on either bus. The input of MAR is connected to the internal bus and it's output is connected to the external bus.

2. Name two special purpose registers.

Index register
Stack pointer

3. Define data path.

The registers, the ALU, and the interconnecting bus are collectively referred to as the data path.

4. Define processor clock.

Processor clock is defined as the time periods in which all operations and data transfer with in the processor take place.

5. What is known as multiphase clocking?

When edge-triggered flip flops are not used, two or more clock signals may be needed to guarantee proper transfer of data. This is known as multiphase clocking.

6. Define MFC.

To accommodate the variability in response time, the processor waits until it receives an indication that the requested read operation has been completed. The control signal used for this purpose is known as memory-function-completed(MFC).

7. What is WMFC?
WMFC if the control signal that causes the processor's control circuitry to wait for the arrival of the MFC signal.

8.What is meant by branch instruction?

A branch instruction is an instruction which replaces the contents of the PC with the branch target address. This address is usually obtained by adding offset X, which is given in the branch instruction is called a branch delay slot.

9. Define register file.

All general purpose registers are combined into a single block called the register file.

10. What are the two approaches used for generating the control signals in proper sequence?

- Hardwired control
- Microprogrammed control

11. What are the factors determine the control signals?

- Contents of the control step counter
- Contents of the instruction register
- Contents of the condition code flag
- External input signals such as MFC & interrupt requests

12. Explain hardwired control.

The control hardwire can be viewed as the state machine that changes from one state to another in every clock cycle, depending on the contents of the instruction register, the condition codes and the external inputs. The outputs of the state machine are the control signals. The sequence of operations carried out by this machine is determined by the writing of the logic elements, hence the name “hardwired”.

13. What are the features of the hardwired control?

A controller that uses this approach can operate at high speed. It has little flexibility and the complexity of the instruction set it can implement is limited.

14. What is micro programmed control?

Micro programmed control is a scheme in which control signals are generated by a program similar to machine language program.

15. What is control word?

A control word is a word whose individual bits represent the various control signals.

16. Define microroutine and microinstruction.

A sequence of control words corresponding to the control sequence of a machine instruction constitutes the microroutine for that instruction and the individual control words in this microroutine are referred to as microinstructions.

17. What is control store?

The microroutines for all the instructions in the instruction set of a computer are stored in a special memory called the control store.

18. What is the draw back of assigning one bit position to each control signals?

Assigning individual bits to each control signal results in long microinstructions because the number of required signals is usually large.
Moreover, only a few bits are set to "1" in any given microinstruction, which means the available bit space is poorly used.

19. Name some register output control signals.

Pc_{out}, MDR_{out}, Z_{out}, $Offset_{out}$, $R1_{out}$, $R2_{out}$, $R3_{out}$ and $TEMP_{out}$.

20. What is vertical organization and horizontal organization?

Highly encoded schemes that use compact codes to specify only a small number of control functions in each microinstruction are referred to as vertical organization. On the other hand, the minimally encoded scheme in which many resources can be controlled with single microinstructions is called a horizontal organization.

21. Compare vertical organization and horizontal organization

Vertical organization	Horizontal organization
• Highly encoded schemes. • Specify only a small number of	Minimally encoded schemes. Many resources can be controlled.

control signals. • Operating speed is high.	Operating speed is low.

22. Explain bit-O-Ring technique.

The micro program shows that branches are not always made to a single branch address. This is a direct consequence of combining simple micro routines by sharing common parts. Consider a point in the microprogram sequencing. At this point, it is necessary to choose between actions required by direct and indirect addressing modes. If the indirect mode is specified in the instruction, then the microinstruction in the location 170 is performed to fetch the operand from the memory. If the direct mode is specified, this fetch must be bypassed by branching immediately to location 171. the most efficient way to bypass microinstruction 170 is to have the preceding branch microinstructions specify the address 170 and then use an OR gate change the least significant bit of this address to '1' if the direct addressing mode is involved. This is known as the bit-O-ring technique for modifying branch address.

23. What is the draw back of micro programmed control?

It leads to a slower operating speed because of the time it takes to fetch microinstructions from the control store.

24. Define emulation.

Given a computer with a certain instruction set, it is possible to define additional machine instructions and implement them with extra micro routines. Emulation allows us to replace obsolete equipment with more up to date machines. If the replacement computer fully emulates the original one, then no software changes have to be made to run existing programs. Thus, emulation facilitates transitions to new computer systems with minimal distribution.

UNIT III

1. Define pipelining.

Pipelining is an effective way of organizing concurrent activity in a computer system. The processor executes the program by fetching and executing instructions, one after another.

2. What are the major characteristics of a pipeline?

Ans: The major characteristics of a pipeline are:
a) Pipelining cannot be implemented on a single task, as it works by splitting multiple tasks into a number of subtasks and operating on them simultaneously.
b) The speedup or efficiency achieved by suing a pipeline depends on the number of pipe stages and the number of available tasks that can be subdivided.
c) If the task that can be subdivided has uneven length of execution times, then the speedup of the pipeline is reduced.
d) Though the pipeline architecture does not reduce the time of execution of a single task, it reduces the overall time taken for the entire job to get completed.

3. What are the types of pipeline hazards?

Ans: The various pipeline hazards are:

1. Data hazard
2. Structural Hazard
3. Control Hazard.

4. What is a pipeline hazard?
Ans: Any condition that causes the pipeline to stall is called hazard. They are also called as stalls or bubbles.

5. Name the four steps in pipelining.

Fetch	: Read the instruction from the memory.
Decode	: Decode the instruction and fetch the source operand.
Execute	: Perform the operation specified by the instruction.
Write	: Store the result in the destination location.

6. What is the use of cache memory?

The use of the cache memories solves the memory access problem. In particular, when a cache is included on the same chip as the processor, access time to cache is usually the same as the tine needed to perform other basic operations inside the processor. This makes it possible to divide instruction fetching and processing into steps

that are more or less equal in duration. Each of these steps is performed by a different pipeline stages, and the clock period is chosen to correspond to the longest one.

7. What is data hazard?

Any condition that causes the pipeline to stall is called a hazard. A data hazard is any condition in which either the source or destination operands of instruction are not available at the time expected in the pipeline. As a result some operation has to be delayed, and the pipeline stalls.

8. What are instruction hazards?

The pipeline may also be stalled because of a delay in the availability of an instruction. For example, this may be a result of a miss in the cache, requiring the instruction to be fetched from the main memory. Such hazards are often called control hazards or instruction hazards.

9. What are called stalls?

An alternative representation of the operation of a pipeline in the case of a cache miss gives the function performed by each pipeline stage in each clock cycle. The periods in which the decode unit, execute unit and the write unit are idle are called stalls. They are also referred to as bubbles in the pipeline.

10. What is structural hazard?

Structural hazard is the situation when two instructions require the use of a given hardware resource at the same time. The most common case in which this hazard may arise is in access to memory.

11. What is said to be side effect?

When a location other than one explicitly named in an instruction as a destination operand is affected, the instruction is said to have a side effect.

12. What is dispatch unit?

A separate unit which we call the dispatch unit takes instructions from the front of the queue and sends them to the execution unit. The dispatch unit also performs the decoding function.

13. What is branch folding?

The instruction fetch unit has executed the branch instruction concurrently with the execution of other instructions. This technique is referred to a branch folding.

14. What are the two types of branch prediction techniques available?

Ans: The two types of branch prediction techniques are

1) Static branch prediction
2) Dynamic branch prediction

15. What is delayed branching?

A technique called delayed branching can minimize the penalty incurred as a result of conditional branch instructions. The idea is simple. The instructions in the delay slots are always fetched. Therefore, we would like to arrange for them to be fully executed whether or not the branch is taken. The objective is to be able to place useful instructions in these slots. If no useful instructions can be placed in the delay slots, these slots must be filled with NOP instructions.

16. Define speculative execution.

Speculative execution means that instructions are executed before the processor is certain that they are in the correct execution sequence. Hence, care must be taken that no processor registers or memory locations are updated until it is confirmed that these instructions should indeed be executed. If the branch decision indicates otherwise, the instructions and all their associated data in the execution units must be purged, and the correct instruction fetched and executed.

17. What is called static and dynamic branch prediction?

The branch prediction decision is always the same every time a given instruction is executed. Any approach that has this characteristic is called static branch prediction. Another approach in which the prediction decision may change depending on execution history is called dynamic branch prediction.

18. What are condition codes?

In many processors, the condition code flags are stored in the processor status register. They are either set are cleared by many instructions, so that they can be tested by subsequent conditional branch instructions to change the flow of program execution.

19. What are superscalar processors?

Several instructions start execution in the same clock cycle, and the processor is said to use multiple issue. Such processors are capable of achieving an instruction execution throughput of more than one instruction per cycle. They are known as superscalar processors.

20. What is imprecise and precise exception?

Situation in which one or more of the succeeding instructions have been executed to completion is called imprecise exception. Situation in which all subsequent instructions that may have been partially executed are discarded. This is called a precise exception.

21. What is commitment unit?

When out-of-order execution is allowed, a special control unit is needed to guarantee in-order commitment. This is called the commitment unit. It uses queue called the recorder buffer to determine which instruction should be committed next. Instructions are entered in the queue strictly in program order as they are dispatched for execution.

22. What is a deadlock?

A deadlock is a situation that can arise when two units, A and B use a shared resource. Suppose that unit B cannot complete its task until unit A completes its task. At the same time, unit B has been assigned a resource that unit A needs. If this happens, neither unit can complete its task. Unit A is waiting for the resource it needs, which is being held by unit B at the same time, unit B is waiting for unit A to finish before it can release that resource.

UNIT IV

1. What is the maximum size of the memory that can be used in a 16-bit computer and 32 bit computer?

The maximum size of the memory that can be used in a 16-bit computer is 2 memory locations. The maximum size of the memory that can be used in a 32-bit computer is 2 memory locations.

2. Define memory access time?

The time required to access one word is called the memory access time. Or It is the time that elapses between the initiation of an operation and the completion of that operation

3. Define memory cycle time?

It is the time delay required between the initiations of two successive memory operations.

Eg. The time between two successive read operations.

4. When is a memory unit called as RAM?

A memory unit is called as RAM if any location can be accessed for a read or writes operation in some fixed amount of time that is independent of the locations address.

5. What is MMU?

MMU is the Memory Management Unit. It is a special memory control circuit used for implementing the mapping of the virtual address space onto the physical memory.

6. Define memory cell?

A memory cell is capable of storing one bit of information. It is usually organized in the form of an array.

7. What is a word line?

In a memory cell, all the cells of a row are connected to a common line called as word line.

8.Define static memories?

Memories that consists of circuits capable of retaining their state as long as power is applied is called static memories

9.What are the characteristics of semiconductor RAM memories?

- They are available in a wide range of speeds.
- Their cycle time range from 100ns to less than 10ns.
- They replaced the expensive magnetic core memories
- They are used for implementing memories.

10.Why SRAM are said to be volatile?

Because their contents are lost when power is interrupted. So SRAM are said to be volatile.

11.What are the characteristics of SRAM?

- SRAM are fast
- They are volatile
- They are of high cost
- Less density

12. What are the characteristics of DRAM?

- Low cost
- High density
- Refresh circuitry is needed

13. Define Refresh Circuits?

It is a circuit which ensures that the contents of a DRAM are maintained when each row of cells are accessed periodically.

14. Define Memory Latency?

It is used to refer to the amount of tile it takes to transfer a word of data to or from the memory.

15. What is asynchronous DRAM?

In asynchronous DRAM, the timing of the memory device is controlled asynchronously. A specialized memory controller circuit provides the necessary control signals RAS and CAS that govern the timing. The processor must take into account the delay in the response of the memory such memories are asynchronous DRAM.

16. What is synchronous DRAM?

Synchronous DRAM's are those whose operation is directly synchronized with a clock signal.

17. Define Bandwidth?

When transferring blocks of data, it is of interest to know how much time is needed to transfer an entire block, since blocks can be variable in size it is useful to define performance measure in terms of number of bits or bytes that can be transferred in one second. This measure is often referred to as the memory bandwidth.

18. What is double data rate SDRAM?

Double data rates SDRAM are those which can transfer data on both edges of the clock and their bandwidth is essentially doubled for long burst transfers.

19. Want is mother board?

Mother Board is a main system printed circuit board which contains the processor. It will occupy an unacceptably large amount of space on the board.

20. What are SIMM and DIMM?

SIMM are Single In-Line Memory Module.DIMM is Dual In-Line Memory Modules. Such modules are an assembly of several memory chips on a separate small board that plugs vertically into a single socket on the motherboard.

21. What is memory controller?

A memory controller is a circuit which is interposed between the processor and the dynamic memory. It is used for performing multiplexing of address bits. It provides RAS-CAS timing. It also sends R/W and CS signals to the memory. When used with DRAM chips, which do not have self refreshing capability, the memory controller has to provide all the information needed to control the refreshing process.

22. Differentiate static RAM and dynamic RAM?

S.NO	STATIC RAM	DYNAMIC RAM
1	They are fast	They are slow
2	They are very expensive	They are less expensive
3	They retain their state indefinitely	They do not retain their state indefinitely
4	They require several transistors	They require less no transistors
5	Low density	High density

23. What is RAM Bus technology?

The key feature of RAM bus technology is a fast signaling method used to transfer information between chips. Instead of using signals that have voltage levels of either 0 or V supply to represent the logic values the signals consists of much smaller voltage swings around a reference voltage, vref, small voltage swings make it possible to have short transition times, which allows for a high speed of transmission.

24. What are RDRAM?

RDRAM are Rambus DRAM. Rambus require specially designed memory chips. These chips use cell arrays based on the standard DRAM technology. Multiple banks of cell arrays are used to access more than one word at time. Circuitry needed to interface to the Rambus channel is included on the chip. Such chips are known as RDRAM.

25. What are the special features of Direct RDRAM?

- It is a two channel Rambus
- It has 18 data lines intended to transfer two bytes of data at a time
- There are no separate address lines

26. What are RIMM?

RDRAM chips can be assembled into larger modules called RIMM. It can hold up to 16 RDRAM

27. Define ROM?

It is a non-volatile memory. It involves only reading of stored data.

28. What are the features of PROM?

- They are programmed directly by the user.
- Faster

- Less expensive
- More Flexible

29. Why EPROM chips are mounted in packages that have transparent window?

Since the erasure requires dissipating the charges trapped in the transistors of memory cells. This can be done by exposing the chip to UV light.

30. What are disadvantages of EPROM?

The chip must be physically removed from the circuit for reprogramming and its entire contents are erased by the UV light.

31. What are advantages and disadvantages of using EEPROM?

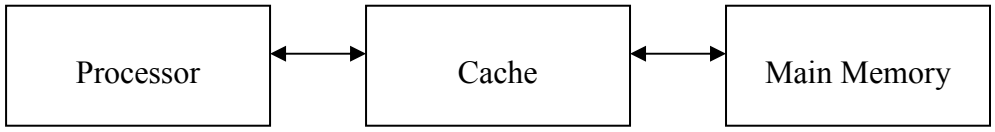
The Advantages are that EEPROM do not have to be removed for erasure. Also it is possible to erase the cell contents selectively. The only disadvantage is that different voltages are needed for erasing, writing and reading the stored data.

32. Differentiate Flash devices and EEPROM devices.

S.NO	FLASH DEVICES	EEPROM DEVICES
1	It is possible to read the contents of a single cell, but it is only possible to write an entire block of cells	It is possible to read and write the contents of single cell
2	Greater density which leads to higher capacity	Relatively lower density
3	Lower cost per bit	Relatively more cost
4	Consumes less power in their operations and makes it more attractive for use in portable equipments that is battery driven	Consumes more power

33. What is cache memory?

It is a small, fast memory that is inserted between large, slower main memory and the processor. It reduces the memory access time



34. Define Flash Memory.

It is an approach similar to EEPROM technology. A flash cell is based on a single transistor controlled by trapped charge just like an EEPROM cell.

35. What is locality of reference?

Analysis of program shows that many instructions ion localized areas of the program are executed repeatedly during some time period, and the remainder of the program, accessed relatively infrequently. This is referred to as locality of reference. This property leads to the effectiveness of cache mechanism.

36. What are the two aspects of locality of reference? Define them.

Two aspects of locality of reference are temporal aspects and spatial aspect.

- Temporal aspect is that a recently executed instruction is likely to be executed again very soon.
- The spatial aspect is that instructions in close proximity to recently executed instructions are also to be executed soon

37. Define cache line.

Cache block is used to refer to a set of contiguous address location of some size. Cache block is also referred to as cache line.

38. What are the two ways in which the system using cache can proceed for a write operation?

- Write through protocol technique
- Write–back or Copy–back protocol technique

39. What is write-through protocol?

For a write operation using write-through protocol during write-hit: The cache location and the main memory location are updated simultaneously.

For a write-miss: For a write-miss, the information is written directly to the main memory

40. What is write-back or copy-back protocol?

For a write operation using this protocol during write-hit: the technique is to update only the cache and to mark it as updated with an associated flag bit, often called the dirty or modified bit. The main memory location of the word is updated later, when the block containing this marked word is to be removed from the cache to make room for a new block.

For a write-miss: the block containing the addressed word is first brought into the cache, and then the deserved word in the cache is overwritten with the new information.

41. What is load-through or early restart?

When a read miss occurs for a system with cache the required word may be sent to the processor as soon as it is read from the main memory instead of loading in to the cache. This approach is called load through or early restart and it reduces the processor's waiting period.

42. What are the mapping techniques?

→ Direct mapping
→ associative mapping
→ Set associative mapping

43. What is hit?

A successful access to data in cache memory is called hit.

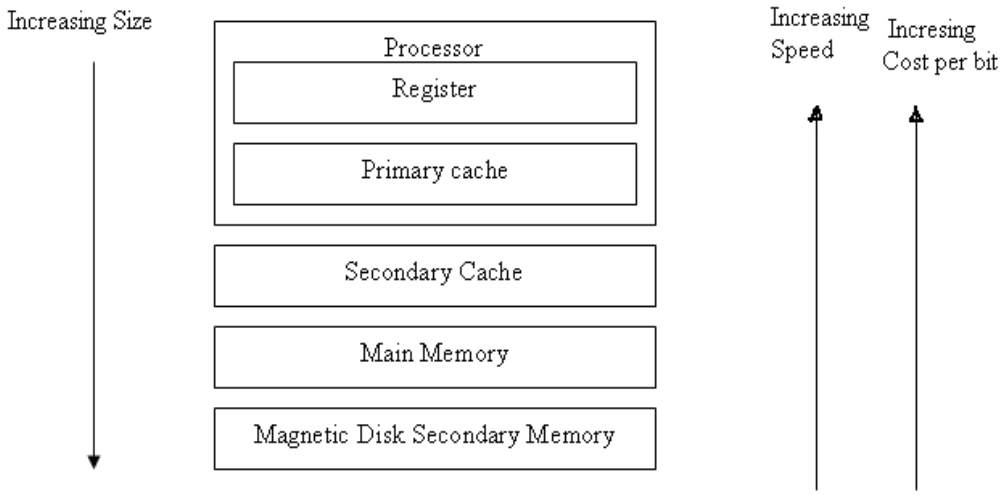
44. Define hit rate?

The number of hit states as a fraction of all attempted access.

45. What are the two ways of constructing a larger module to mount flash chips on a small card?

→ Flash cards
→ Flash drivers.

46. Describe the memory hierarchy.



48. Define miss rate?

It is the number of misses states as a fraction of attempted accesses.

49. Define miss penalty?

The extra time needed to bring the desired information into the cache is called miss penalty.

50. Define access time for magnetic disk.

The sum of seek time and rotational delay is called as access time for disks.

Seek Time:

Seek time is the time required to move the read/write head to the proper track.

Rotational latency:

Rotational latency is the amount of time that elapses after the head is positioned over the correct track until the stating position of the addressed sector passes under the read/write head.

51. What is phase encoding or Manchestor encoding?

It is the technique for combining clock information with data. It is a scheme in which changes in magnetization occur for each data bit. It's disadvantage is poor bit-storage density.

52. What is the formula for calculating the average access time experienced by the processor?

$T_{avg} = h\,c + (1-h)\,M$

Where

h- Hit Rate
M – Miss Penalty
C – Time to access information in the cache.

53. What is the formula for calculating the average access time experienced by the processor in a system with two levels of cache?

$T\ avg = h_1\ c_1 + (1-h_1)\ h_2\ c_2 + (1-h_1)\ (1-h_2)\ M$

h 1 – Hit rate in L1 cache
h 2 – Hit rate in L2 cache
c 1 – Time to access information in the L1 cache
c 2 – Time to access information in the L2 cache

54. What are prefetch instructions?

Prefetch instructions are those instructions which can be inserted into a program either by the programmer or by the compiler.

55. Define system space.

Management routines are part of the operating system of the computer. It is convenient to assemble the OS routines into a virtual address space.

56. Define user space?

The system space is separated from virtual address space in which the user application programs reside. The letter space is called user space.

57. What are pages?

All programs and date are composed of fixed length units called pages. Each consists of blocks of words that occupy contiguous locations in main memory.

58. What is replacement algorithm?

When the cache is full and a memory word that is not in the cache is referenced, the cache control hardware must decide which block should be removed to create space for the new block that contains the reference word. The collection of rules for making this decision constitutes the replacement algorithm.

59. What is write miss?

During the write operation if the addressed word is not in cache then said to be write miss.

60. What is associative search?

The cost of an associative cache is higher that the cost of a direct mapped cache because of the need to search all 128 bit tag patterns to determine whether a given block is in the cache. A search of this kind is called an associative search.

61. What is virtual memory?

Technique that automatically move program and datablocks into the physical main memory when they are required for execution are called as virtual memory.

62. What is virtual address?

The binary address that the processor used for either instruction or data called as virtual address.

63. What is page frame?

An area in the main memory that can hold one page is called as page frame.

64. What is Winchester technology?

The disk and the read/write heads are placed in a sealed air-filtered enclosure called Winchester technology.

65. What is a disk drive?

The electro mechanical mechanism that spins the disk and moves the read/write heads called disk drive.

66. What is disk controller?

The electronic circuit that controls the operation of the disk called disk controller.

67. What is word count?

The number of words in the block to be transferred.

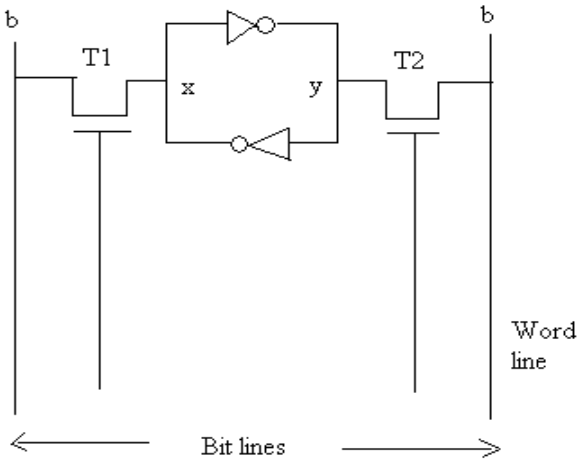
68. What is error checking?

It computes the error correcting code (ECC) value for the data read from the given sector and compares it with the corresponding ECC value read from the disk.

69. What is booting?

When the power is turned on, the OS has to be loaded into the main memory which is taken place as part of a process called booting. To initiate booting a tiny part of main memory is implemented as a nonvolatile ROM.

70. Draw static RAM cell.



UNIT V

1. Why IO devices cannot be directly be connected to the system bus?

Ans: The IO devices cannot be directly connected to the system bus because

i. The data transfer rate of IO devices is slower that of CPU.
ii. The IO devices in computer system has different data formats and work lengths that of CPU.

So it is necessary to use a module between system bus and IO device called IO module or IO system

2. What are the various mechanisms for implementing I/O operations?

- Program controlled I/O
- Interrupts
- DMA

3. What are the major functions of IO system?

Ans: i. Interface to the CPU and memory through the system bus.
ii. Interface to one or more IO devices by tailored data link.

1. What is memory mapped I/O?

When the I/O devices share the same address space, the arrangement is called memory mapped I/O.

2. What is program controlled I/O?

In program controlled I/O the processor repeatedly checks a status flag to achieve the required synchronization between the processor and an input and output device.

4. What is an I/O Interface?

Ans: Input-output interface provides a method for transferring binary information between internal storage, such as memory and CPU registers, and external I/O devices

5. Write the factors considered in designing an I/O subsystem?

Ans:

1. Data Location: Device selection, address of data with in device(track, sector etc)
2. Data transfer: Amount, rate to or from device.
3. Synchronization: Output only when device is ready, input only when data is available.
4. I/O operation: refers to a data transfer between an I/O device and Memory or between an I/O device and CPU.

6. Explain Direct Memory Access.

Ans: A modest increase in hardware enables an IO device to transfer a block of information to or from memory without CPU intervention. This task requires the IO device to generate memory addresses and transfer data through the bus using interface controllers.

7. Define DMA controller.

Ans: The I/O device interface control circuit that is used for direct memory access is known as DMA controller.

8. What is polling?

Ans: Polling is a scheme or an algorithm to identify the devices interrupting the processor. Polling is employed when multiple devices interrupt the processor through one interrupt pin of the processor.

9. What is the need of interrupt controller?

Ans: The interrupt controller is employed to expand the interrupt inputs. It can handle the interrupt requests from various devices and allow one by one to the processor.

10. What are the two independent mechanisms for controlling interrupt request?

At the device end, an interrupt enable bit in a control register determines whether the device is allowed to generate an interrupt request At the processor end, either an

interrupt enable nit in the PS or a priority structure determines whether a given interrupt request will be accepted.

11. What is a Priority Interrupt?

Ans: A priority interrupt is an interrupt that establishes a priority over the various sources to determine which condition is to be serviced first when two or more requests arrive simultaneously.

12. What are vectored interrupts?

To reduce the time involved in the polling process, a device requesting an interrupt may identify itself directly to the processor. Then the processor can immediately start the executing the corresponding ISR. The schemes based on this approach are called vectored interrupts.

13. Define bus.

Ans: When a word of data is transferred between units, all the bits are transferred in parallel over a set of lines called bus. In addition to the lines that carry the data, the bus must have lines for address and control purposes.

14. Define synchronous bus.

Ans: Synchronous buses are the ones in which each item is transferred during a time slot(clock cycle) known to both the source and destination units. Synchronization can be achieved by connecting both units to a common clock source.

15. Define asynchronous bus.

Ans: Asynchronous buses are the ones in which each item being transferred is accompanied by a control signal that indicates its presence to the destination unit. The destination can respond with another control signal to acknowledge receipt of the items.

16. What do you mean by memory mapped I/O?

Ans: In Memory mapped I/O, there are no specific input or output instructions. The CPU can manipulate I/O data residing in interface registers with the same instructions that are used to manipulate memory words i.e. the same set of instructions are used for reading and writing memory can be used to input and output.

17. What is program-controlled I/O?

Ans: In program controlled I/O the processor repeatedly checks a status flags to achieve the required synchronization between the processor and an input and output device.

18. Define interrupt.

Ans: An interrupt is any exceptional event that causes a CPUU to temporarily transfer control from its current program to another program , an interrupt handler that services the event in question.

19. Define exception.
Ans: The term exception is used to refer to any event that causes an interruption

20. What are the different methods used for handling the situation when multiple interrupts occurs?
Ans: 1) Vectores interrupts
2) Interrupt nesting
3) Simultaneous Requests.

21. What is a privileged instruction?
Ans: To protect the operating system of a computer from being corrupted by user programs, certain instructions can be executed only while the processor is in the supervisor mode. These are called privileged instruction.

22. What is bus arbitration?
Ans: it is process by which the next device to become the bus master is selected and bus mastership is transferred to it. There are two ways for doing this:
1. Centralized arbitration
2. Distributed arbitration.

23. What is port? What are the types of port available?

Ans: An I/O interface consists of circuitry required to connect an I/O device to computer bus. One side consists of a data path with its associated controls to transfer data between the interface and I/O device. This is called port. It is classified into:
1) Parallel port
2) Serial port.

24. What is a parallel port?
Ans: A parallel port transfers data in the form a number of bits, typically 8 to 16, simultaneously to or from the device.

25. What is a serial port?
Ans: A serial port transfers and receives data one bit at a time.

26. What is PCI bus?
Ans: The Peripheral component interconnect(PCI) bus is a standard that supports the functions found on a processor bus but in a standardized format that is independent of any particular processor.

27. What is SCSI?
Ans: It is the acronym for small computer system interface. It refers to a standard bus defined ANSI. Devices such as disks are connected to a computer via 50-wire cable, which can be upto 25 meters in length and can transfer data at rate up to 55 megabytes/s.

28. Define USB.

Ans: The Universal Serial Bus(USB) is an industry standard developed to provide two speed of operation called low-speed and full-speed. They provide simple, low cost and easy to use interconnection system.

29. What are the objectives of USB?

- Simple
- Low cost
- Easy to use
- Supports wide range of data transfer characteristics
- Plug and play mode of operation

30. What is time slicing?

With this technique each program runs for a short period called a time slice, and then another program runs for its time slice and so on.

PART – B QUESTIONS

UNIT-I

1. Explain the various addressing modes.

- Register mode
- Absolute mode
- Immediate mode
- Indirect mode
- Indexed mode
- Relative mode
- Auto increment mode
- Auto decrement mode

2. Discuss the following:

(i)Basic operational concept of a computer

- Instructions
- Operational details of processor
- Registers
- Operating steps

(ii)Basic instruction types

- Zero address instruction
- One address instruction
- Two address instruction
- Three address instruction

3. Discuss in detail the various measures of performance of a computer.

- Processor clock
- Pipelining and super scalar operation
- Clock rate
- Instruction set
- Compiler

4. Discuss the following

(i) Instruction execution & straight line sequencing

- Execution steps
- Diagram

(ii) Branching

- Explanation
- Diagram

5. Explain in detail the data transfer between the memory & I/O unit.

- Program controlled I/O
- Flags (SIN, SOUT)
- Buffers (DATAIN, DATAOUT)
- Coding
- Diagram

6. Explain the various functional units of a computer

- Input unit
- Output unit
- ALU
- CU
- MU

UNIT-II

1. Give the basic organization of a micro programmed control unit. Draw a flowchart of a
Micro routine for the instruction Add src, Rdst.

- Diagram for basic organization
- Explanation
- Flowchart for Add src, Rdst

2. Describe the micro programmed control unit in detail.
Hints: A micro programmed control unit is built around a storage unit is called a control store where all the control signals are stored in a program like format. The control store stores a set of micro programs designed to implement the behavior of the given instruction set.
Refer page no. 429-445

3. Explain the organization of a Hardwired control unit. Mention its advantages and disadvantages.

- Diagram for basic organization
- Explanation
- Advantages
- Disadvantages

4. Describe the Hardwired control method for generating the control signals
Hints: Hard-wired control can be defined as sequential logic circuit that generates specific sequences of control signal in response to externally supplied instruction
Refer page no. 425- 429
5. Draw the organization of a single bus processor and give the control sequences for fetching a word from memory, storing a word in memory, executing a complete instruction and unconditional branch.

- Diagram
- Control sequences

6. Explain the multiple bus organization structure with neat diagram.
Hints: The multiple bus organization is using more buses instead of one bus to reduce the number of steps needed and to provide multiple paths that enable several transfers to take place in parallel.
Refer page no. 423-425.

UNIT III

1. Explain the various types of hazards in pipelining.

- Instruction hazard
- Data hazard
- Structural hazard

- Control hazard

2. Write notes on super scalar operation?

- Explanation
- Diagram

3. Give the organization of the internal data path of a processor that supports a 4-stage pipeline for instructions and uses a 3- bus structure and discuss the same.
Hints: The speed of execution of programs can be improved by arranging the hardware so that more than one operation can be performed at the same time.
Explain about the 4- stage pipeline.
Refer page no. 4556-459
For 3- bus structure refer page no. 479-481.

4. What is pipelining? What are the various hazards encountered in pipelining? Explain in detail.
Hints: The major characteristics of a pipeline are:
a) Pipelining cannot be implemented on a single task, as it works by splitting multiple tasks into a number of subtasks and operating on them simultaneously.
b) The speedup or efficiency achieved by suing a pipeline depends on the number of pipe stages and the number of available tasks that can be subdivided.
c) If the task that can be subdivided has uneven length of execution times, then the speedup of the pipeline is reduced.
d) Though the pipeline architecture does not reduce the time of execution of a single task, it reduces the overall time taken for the entire job to get completed.
The various pipeline hazards are:

1. Data hazard
2. Structural Hazard
3. Control Hazard.

Refer page no. 459-476.

UNIT-IV

1. Write notes on semiconductor RAM memories

- Internal organization of memory chips
- Static memories
- Asynchronous DRAMs
- Synchronous DRAMs

2. Write notes on various types of ROMs.

- ROM
- PROM
- EPROM

- EEPROM
- Flash memory

3. What are the various types of cache mapping mechanisms? Explain in detail.

- Direct mapping
- Associated mapping
- Set associative mapping
- Explanation

4. Describe the three mapping techniques used in cache memories with suitable Example.

Hints: The cache memory is a fast memory that is inserted between the larger slower main memory and the processor. It holds the currently active segments of a program and their data.

i) Associative mapping.
ii) Direct mapping.
iii) Set-associative mapping

Refer page no. 314-325

5. Explain with neat diagram the internal organization of bit cells in a memory chip.

Hints: Memory cells are usually organized in the form of an array, in which each cell is capable of storing one bit of information. Each row consists a memory word, and all cells of a row are connected to a common line referred to as word line, which is driven by he address decoder on the chip.
Refer Page no. 295-297.

6. Discuss the virtual memory management technique in detail

Hints: The data is to be stored in physical memory locations that have addresses different from those specified by the program. The memory control circuitry translates the address specified by the program into an address that can be used to access the physical memory.
Refer page no. 337-343

7. Explain the various secondary storage devices in detail.

Hints: The various secondary storage devices are:
1. Magnetic hard disks
2. Optical disks
3. Magnetic tape systems Refer page no. 344-359

8. What is memory interleaving? Explain with neat diagram.

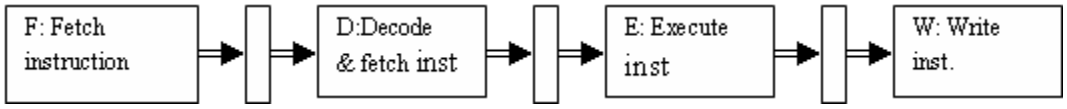
Hints: The main memory of a computer is structure as a collection of physically separate modules each with its own address buffer register and data buffer register, memory access operations may proceed in more than one module at the same time. Thus the aggregate rate of transmission of words to and from the main memory system can be increased.

Refer page no. 330-331

UNIT-V

1. Describe the data transfer method using DMA.

Hints: A modest increase in hardware enables an IO device to transfer a block of information to or from memory without CPU intervention. This task requires the IO device to generate memory addresses and transfer data through the bus using interface controllers.



Refer page no. 234-240.

2. Explain about the interrupts in detail

Hints: An interrupt is any exceptional event that causes a CPUU to temporarily transfer control from its current program to another program , an interrupt handler that services the event in question.

Refer page no. 208-221.

3. Explain the different types of buses with neat diagram.

Hints: When a word of data is transferred between units, all the bits are transferred in parallel over a set of lines called bus. In addition to the lines that carry the data, the bus must have lines for address and control purposes.The different types of buses are:
1. Synchronous Buses:
Synchronous buses are the ones in which each item is transferred during a time slot(clock cycle) known to both the source and destination units. Synchronization can be achieved by connecting both units to a common clock source.
2. Asynchronous buses
Asynchronous buses are the ones in which each item being transferred is accompanied by a control signal that indicates its presence to the destination unit. The destination can respond with another control signal to acknowledge receipt of the items.

Refer page no. 241-247

4. Explain the various interface circuits.

Hints: An I/O interface consists of circuitry required to connect an I/O device to computer bus. One side consists of a data path with its associated controls to transfer data between the interface and I/O device. This is called port. It is classified into:
1) Parallel port

2) Serial port.
Refer page no. 248-259.

5. Explain in details the various standard I/O interfaces.

Hints: The various standard I/O interfaces are:
1. The Peripheral component interconnect(PCI) bus is a standard that supports the functions found on a processor bus but in a standardized format that is independent of any particular processor
2. It is the acronym for small computer system interface. It refers to a standard bus defined ANSI. Devices such as disks are connected to a computer via 50-wire cable, which can be upto 25 meters in length and can transfer data at rate up to 55 megabytes/s.
3. The Universal Serial Bus(USB) is an industry standard developed to provide two speed of operation called low-speed and full-speed. They provide simple, low cost and easy to use interconnection system.
Refer Page no. 259-281.

6. Explain the various methods available to handle multiple devices using interrupts?

- Vectored interrupt
- Interrupt nesting
- Simultaneous requests

7. Write notes on interrupts in operating system?

- Explanation

8. Explain DMA and the different types of bus arbitration mechanisms.

- Diagram
- Explanation
- Centralized arbitration
- Decentralized arbitration
-

9. Explain synchronous and asynchronous bus.

- Explanation
- Diagram

10. Write notes on the following

i.PCI
ii.SCSI
iii.USB

- Explanation
- Diagram

B.E./B.Tech. DEGREE EXAMINATION,NOVEMBER/DECEMBER 2007.

Fourth Semester

(Regulation 2004)

CS1251- COMPUTER ARCHITECTURE

Time:Three hours Maximum:100 marks

Answer ALL questions.

PART A-(10*2=20 marks)

1. **A memory byte location contains the pattern 00101100.What does this pattern represent when interpreted as a number? What does it represent as an ASCII Code?**

   Interpreted number is 44

   ACCII code is NULL/idle

2. **What is the information conveyed by addressing modes?**

   The information conveyed by the addressing mode is to specify the location of an operand in an instruction

3. **Draw the full Adder circuit using two half adders.**

4. **What are the various ways of representing signed integers in the system?**

5. **What are the advantages and disadvantages of hardwired and micro programmed control?**

   Advantages of hardwired control

   i.operate at high speed

   ii. each state of this counter corresponds to one control step

   disadvantages

   i.little flexibility

ii.complexity of the instruction set can implement is limited

advantages of microprogram control

i. control signals are generated by program itself

ii.high flexibility

disadvantages

i.slower operating speed

6. What is data hazard in pipelining? What are the solutions?

A data hazard is a situation in which the pipeline is stalled because the data to be operated on are delayed for some reason.

The solution for data hazard is

i.operand forwading

ii. handled by software

iii. to stall

7. What is virtual memory? How is it implemented?

A technique that automatically move program and data blocks into the physical main memory when they are required for execution. This memory when they are required for execution. This memory is termed as virtual memory. And it is implemented by MMU.

8. What will be the width of address and data buses for a 512k*8 memory chip?

Width of address bus 19

Data bus 8

9. Why do we need DMA?

DMA is used to transfer the block of data directly between an external device and the main memory without the continuous intervention by the processor.

10. What is the difference between subroutine and interrupt service routine?

Subroutine or the sub program is the routine which could be called by another subroutine or main routine under program control.

Interrupt service routine is called automatically on the occurance of an interrupt which is predefined.

PART B-(5*16=80marks)

11 (a) (i) Explain how the processor is interfaced with the memory with a neat block diagram and explain how they communicate. (10)

Page No: 7

(ii) What do you know about bit,bytes,nibbles and word?What are big-endian and little-endian assignments of addresses? (6)

Page No: 33

OR

(b) (i) Write notes on instruction formats. (4) **Page No: 37**

(ii) List the various addressing modes.Give a brief explanation of each of them with an example. (8) **Page No: 68**

(iii) Describe the organization of a stack. (4) **Page No: 68**

12. (a) (i) Design a 4-bit carry –look ahead adder and explain its operation with an example. (8) **Page No: 372**

(ii) Design a binary multiplier using sequential adder.Explain its operation (8) **Page No: 376**

OR

(b) (i) Write about the CSA method of fast multiplication.prove how it is faster with an example. (8) **Page No: 383**

(ii) Draw the circuit for integer division and explain(8)
Page No: 390

13. (a) (i) Explain the instructon cycle highlighting the sub-cycles and sequence of steps to be followed.(8)

(ii) Draw the single bus and three bus organization of the data path inside a processor. (4) **Page No: 412**

(iii) Describe the organization of micro programmed control unit. (4) **Page No: 429**

OR

(b) (i) Design a 4-stage instruction pipeline and show how its performance is improved over sequential execution. (8)

Page No: 454

(ii) Highlight the solutions of instruction hazards. (8)
Page No: 465

14. (a) (i) Write notes on static memories. (8)
Page No: 297

(ii) Explain the concept of memory hierarchy (8)

OR

(b) (i) Write notes on :

(i) ROM Technologies. **Page No: 310**
(ii) Memory Inter Leaving. **Page No: 330**
(iii) Set associative mapping of cache. **Page No: 318**
(iv) RAID Disk arrays. **Page No: 351**

15. (a) (i) Explain how I/Odevices can be interfaced with a block diagram.
Page No: 204 (8)

(ii) How do you connect multiple I/Odevices to a processor using interrupts?Explain with suitable diagrams. (8)
Page No: 208

OR

(b) Write notes on:

(i) DMA. **Page No: 239**
(ii) Bus Arbitration. **Page No: 237**
(iii) Printer processor Communication. **Page No: 251**
(iv) USB. **Page No: 272**

B.E./B.Tech. DEGREE EXAMINATION,MAY/JUNE 2007.

Fourth Semester

(Regulation 2004)

CS1251- COMPUTER ARCHITECTURE

Time:Three hours Maximum:100 marks

Answer ALL questions.

PART A-(10*2=20 marks)

1. Why data bus is bidirectional and address bus is unidirectional in most microprocessors?

The data bus is bidirectional because the data bus has to transfer data between the CPU and memory/I/O device, whereas the address bus is used to send out memory address from the CPU , hence it is unidirectional.

2. **What are limitations of assembly language?**

   i.it is converted to machine language using assembler which is time consuming when compared with machine language.

   ii.it is difficult to solve the complex problems

   iii.a set of symbolic names and rules has to be followed

3. **Why floating point number more difficult to represent and process than integer?**

In floating point numbers we have to represent any number in three fields sighn, exponent and mantissa. The IEEE 754 standard gives the format for these fields and according to the format th numbers are to be represented. In case of any process we have to consider mantissa and exponent separately. Therefore, floating point numbers are more difficult to represent and process than integer.

4. **Draw a full adder circuit and give the truth table.**

5. **Define pipeline speedup.**

   S(m)=T(l)/T(m)

   Where T(m) is the execution time for some target workload on an m-stage pipeline.

   T(l) is the execution time for some workload an a similar non pipelined processor.

6. **State the differences between hardwired and micro programmed control unit.**

Hardwired control	Microprogrammed control
-- It is implemented using the gates, flip flop and hardwired circuits.	--It is implemented using the micro program stored in the control memory.
--No control memory is used.	--Control memory is used.
--Execution is faster.	--Execution is slower.

--Modification is difficult.	--Modification is simple by modifying the
--RISC machines	micro program in the control memory.
	--CISC Machines.

7. **List the factors that determine the storage device performance**.

   i.Access time

   ii.Cycle time

   iii.Transfer Rate.

8. **How many 128*8 RAM chips are needed to provide a memory capacity of 2048 bytes?**

   128*8=1024 bytes.

   One 128*8 chip can store 1024 bytes, hence to have memory capacity of 2048 bytes we need two 128*8 RAM chip.

9. **Why does DMA have priority over the CPU when both request a memory transfer?**

   The data transfer monitored by DMA controller which is known as DMA channel. The CPU is involved only at the beginning and end of the transfer, when the CPU wishes to read or write a block of data, it issues a command to DMA Channel by sending read/write operation, address of I/O, number of words to be read or written, hence DMA have priority over the CPU when both request a memory transfer.

10. **What is the advantage of using interrupt initiated data transfer over transfer under program control without interrupt?**

    In the interrupt initiated data transfer, the processor identifies the request and transfer the control ISR to perform the task and its resumes back with the useful task whereas, the processor has to waste its time by performing all the task, for example when a print command is given in the interrupt initiated , it gives control over to ISR and resumes the work back where as without interrupt the processor has to wait until the print document is transferred to the printer.

PART B-(5*16=80 marks)

11. (a) (i) What is a stack?illustrate the use of stack in subroutine processing with suitable diagram. (8)
Page No: 68

(ii). Describe different types of addressing modes in detail (8)
Page No: 48

OR

(b). (i) Briefly explain any six I/O operations with an example (9)
Page No: 64

(ii) Illustrate memory read and write operations. (7)
Page No: 65

12. (a) (i). Give the block diagram of the hardware implementation of addition and subtraction of signed number and explain the operation with flowchart. (10) **Page No: 368**

(ii) Explain the representation of floating point numbers in detail.
Page No: 393 (6)

OR

(b) (i). Design a multiplier that multiplies two 4 bit numbers. (8)
Page No: 376

(ii) Describe the algorithm for integer division with suitable example.
Page No: 390 (8)

13 (a) (i) Explain the execution an instruction with diagram. (8)
Page No: 421

(ii) Explain the functions of a six segment pipeline and draw a space diagram for a six segment pipeline showing the time it takes to process eight tasks. (8)
Page No: 454

OR

(b) (i) Explain how the performance of the instruction pipeline can be improved. (10) **Page No: 465**

(ii) Explain multiple bus organization in detail.(6)

14. (a) (i). What is virtual memory?Explain how the logical addres is translated into physical address in the virtual memory system with a neat diagram. (10)
Page No: 337

(ii) Describe the organization of a typical RAM chip. (6)

Page No : 295

OR

(b) (i) Explain the organization of magnetic disk in detail (6)
Page No: 344

(ii) A digital computer has a memory unit of 64 k*16 and a cache memory of 1 k words.The cache uses direct mapping with a block size of four words.How many bits are there in the tag,index,block and word fields of the address format ?How many blocks can the cache accommodate? (10)

15. (a) (i) Design a parallel priority interrupt hardware for a system with eight interrupt sources. (8)
Page No: 208

(ii). describe the functions of SCSI with a neat diagram (8)
Page No: 266

OR

(b) (i) What is the importance of an I/O interface compare features of SCSI and PCI interfaces. (6)
Page No: 259

(ii) What are different input and output signals of DMA controller? Why are the read and write control signals are bidirectional?Under what condition and for what purpose they are used as inputes and outputs? (10)
Page No: 234

B.E./B.Tech. DEGREE EXAMINATION,APRIL/MAY 2008.

Fourth Semester

(Regulation 2004)

CS1251- COMPUTER ARCHITECTURE

Time:Three hours Maximum:100 marks

Answer ALL questions.

PART A-(10*2=20 marks)

1. **What are tri-state gate?**
2. **Why is the data bus in most microprocessors bidirectional while the address bus is unidirectional?**

   Data Bus: These lnes are used to send data to memory via output ports and to receive data from memory via input ports. Therefore, data bus lines are bi-directional.

   Address Bus: On these lines the CPU send out the address of the memory location or I/O port that is to be written to or read from. Here, the communiation is one-way, the address is send from CPU to memory and I/O port and hence these lines are unidirectional.

3. **Perform 1010100 – 1000100 using 1's and 2's complement.**

4. **Define underflow and overflow.**

Underflow: If the result the arithmetic operation involving n-bit numbers is too small to represent by n-bits, underflow is said to occur.

Overflow: If the result of an arithmetic operation is outside the representable range, then overflow is said to occur.

5. **What is pipelining and what are the advantages of pipelining?**

Pipelining is a technique of decomposing a sequential process into suboperations, with each subprocess being executed in a special dedicated segment that operates concurrently with all other segments.

Advantages:
i. Increases computer processing capability
ii. Increased throughput

6. **What is the difference between hardwired control and micro programmed control?**
7. **List the differences between static RAM and dynamic RAM.**

SRAM: Static Random Access Memory. It tends to be faster. They require no refreshing.

DRAM: Dyanamic Random Access Memory. Data is stored in the form of charges. So continuous refreshing is needed.

8. **Define the terms : spatial locality and temporal locality.**

Spatial Locality: The spatial aspect means that instructions in close proximity to a recently executed instruction are closely likely to be executed soon.

Temporal Locality: Temporal means that instructions that are recently executed, are likely to be executed again very soon.

9. What factors influences the bus design decisions?

1. Data Location: Device selection, address of data with in device(track, sector etc)
2. Data transfer: Amount, rate to or from device.
3. Synchronization: Output only when device is ready, input only when data is available.
4. I/O operation: refers to a data transfer between an I/O device and Memory or between an I/O device and CPU.

10. What is priority interrupt?

A priority interrupt is an interrupt that establishes a priority over the various sources to determine which condition is to be serviced first when two or more requests arrive simultaneously.

PART B – (5×16=80 marks)

11. (a) (i) With a neat diagram explain Von-Neumann computer architecture. (12)

(ii) What are the major instruction design issues? (4)

Page No: 37

Or

(b) (i) Explain various instruction formats in detail. (10)

Page No: 37

(ii) What is a stack and what are the operations on stack? Give any three applications of stack. (6)

Page No: 68

12. (a) (i) Design a 4-bit binary adder/subtractor and explain its functions.

Page No: 372 (8)

(ii) Give the algorithm for multiplication of signed 2's complement numbers and illustrate with an example. (8)

Page No: 380

OR

(b) (i) Design an array multiplier that multiplies two 4-bit numbers and explain its operation. (8)

Page No: 376

(ii) Write the algorithm for division of floating point numbers and illustrate with an example. (8)

13. (a) (i) What is branch hazard? Describe the methods for dealing with the branch hazards. (10)
Page No: 465

(ii) With a suitable diagram describe the sequence of micro operations involved in fetching and executing a typical instruction. (6)

OR

(b) What is data hazard? Explain the methods for dealing with the data hazards. (16) **Page No : 461**

14. (a) (i) Describe the functional characteristics that are common to the devices used to build main and secondary computer memories. (6)
Page No: 295

(ii) Explain various mechanisms of mapping main memory address into cache memory addresses. (10)
Page No: 314

Or

(b) (i) Explain how the virtual address is converted into real address in a paged virtual memory system. (10) **Page No: 337**

(ii) Describe the working principle of a typical magnetic disk. (6)
Page No: 344

15. (a) Draw the typical block diagram of a DMA controller and explain how it is used for direct data transfer between memory and peripherals. (16)
Page No: 234

Or

(b) (i) Describe the working principles of USB. (8)
Page No: 272

(ii) Briefly compare the characteristics of SCSI with PCI. (8)
Page No: 261 & 266

B.E./B.Tech. DEGREE EXAMINATION,NOVEMBER/DECEMBER 2006.
Fourth Semester
(Regulation 2004)
CS1251-COMPUTER ARCHITECTURE

Time:Three hours Maximum:100 marks

Answer ALL questions.
PART A-(10*2=20 marks)

1. **What is a bus? What are the different buses in a CPU?**

Ans: A group of lines that serve as a connecting path for several devices is called bus.

The different buses in a CPU are

- Data bus
- Address bus
- Control bus

2. **What are the four basic types of operations that need to be supported by an instructor set?**

i. Data transfer between memory and the processor register.

ii. Arithmetic and logic operations on Data.

iii. Program sequencing and control

iv. I/O transfer

3. **Draw the symbolic representation of the full adder and give the expression for the sum.**

4. **In confirming to the IEEE standard mention any four situations under which a processor sets exception flag.**

i. Underflow

ii. Overflow

iii. Divide by zero

iv. Invalid

5. What are the address-sequencing capabilities required in a control memory?

i. Increamenting the control address register

ii. Unconditional branch as specified by address field of the microinstruction.

iii. Conditional branch depending on status bits in register of computer

iv. A facility for sub-routine calls and retuns.

6. What is meant by super scalar processor?

Super scalar processors are designed to exploit more instruction level parallelism in user programs. This means that multiple functional units are used. With such an arrangement it is possible to start the execution of several instruction in every clock cycle. This mode operation is called super scalar execution.

7. What do you understand by Hit ratio?

Whan a processor refers a data item from a cache, if the referenced item is in the cache, then such a reference is called hit. If the referenced data is not in the cache, then it is called miss (or cache miss). Hit ratio is defined as the ratio of number of hits to number of refernces.

$$\text{Hit Ratio} = \frac{\text{No.of Hits}}{\text{Total no.of references}} = \frac{\text{No.of Hits}}{\text{Hits + Misses}}$$

8. Define locality of reference? What are its types?

During the course of execution of a program memory references by the processor for both the instruction and the data tends to cluster. There are two types,

i. Spatial Locality

ii. Temporal Locality

9. What is DMA operations? State its advantages.

In order to transfer bulk amount of data between memory and I/O device without involvement of CPU, the Direct Memory Access technique is used. The advantage is, fasr data transfer.

10. What is the necessity of an interface?

Any device that has to be connected to a CPU require an intrface. Which takes care of the mismatch in speed, data and electrical characteristics between the CPU to the decvice.

PART B-(5*16=80marks)

11. (a) (i) Give the difference instruction formats of a CPU in general. (6)

Page No: 37

(ii) Define addressing mode.Classify addressing modes and explain each type with examples. (10)

Page No: 48

OR

(b) (i) Write an assembly language to find the biggest number among given three numbers (6) **Page No: 58**

(ii) Explain instruction set and instruction sequencing (10). **Page No: 37**

12. (a) (i) What is the advantage in using ripple carry adder (4) **Page No: 385**

(ii) Draw the diagram of a carry look ahead adder and explain the carry lookahead principle. (12) **Page No: 372**

OR

(b) (i) Give the IEEE standard double precision floating point format.(3) **Page No: 394**

(ii) Explain the floating point add/subtract rules.With a detailed flow chart explain how floatin point additional subtraction is performed (13) **Page No: 398**

13. (a) With a neat diagram explain the basic organization of a microprogrammmed control unit.Explain the operation of this control unit with a typical set of micro instructions. (16) **Page No: 429**

OR

(b) (i) Explain the various design methods of hardwired control unit. (8) **Page No: 425**

(ii) Explain the basic concepts of pipelining and comparing it with sequential processing.Draw needed diagrams. (8) **Page No: 454**

14. (a) (i) Draw a neat sketch of memory hierarchy and explain the need of cache memory. (8) **Page No: 314**

(ii) Explain the various mapping functions used for mapping main memory blocks in to cache memory. (8) **Page No: 316**

OR

(b). (i) Explain the virtual memory address translation and TLB with necessary diagram. (10) **Page No: 337**

(ii) Dicuss the concept of memory interleaving and give its advantages. (6) **Page No: 330**

15. (a) (i) Discuss the general steps involved in interrupt driven data transfer. (6) **Page No: 208**

(ii) Explain how DMA transfer is accomplished with a neat diagram (10) **Page No: 234**

OR

(b) Write short notes on:
(i) PCI (8) **Page No: 261**
(ii) Advantages of USR over older I/O bus architectures (8)

B.E./B.Tech. DEGREE EXAMINATION,MAY/JUNE 2006.
Fourth Semester
(Regulation 2004)
CS1251-COMPUTER ARCHITECTURE

Time:Three hours Maximum:100 marks

Answer ALL questions.

PART A-(10*2=20 marks)

1. **Give an example each of zero-address, one address, two-address, and three-address instructions.**
   i. Zero address Instruction: locations of all operands are defined implicitly
   ii. One address Instruction: Add A
   iii. Two address Instruction: Add A , B
   iv. Three address Instruction: Add A , B , C

2. **Which data structures can be best supported using (a) indirect addressing mode (b) indexed addressing mode?**
   (a) Indirect Addressing mode → Pointer data structure
   (b) Indexed Addressing mode → Array data structure

3. **What is the purpose of guard bits used in floating point operations?**

The guard bits are the extra bits which is used to retain the intermediate steps to increase the accuracy in the final result.

4. **Give the booth's recording and bit pair recording of the number 1000111101000101.**

5. **Why is the Wait-For-Memory-Function-Completed step needed when reading from or writing to the main memory?**

WMFC step is required for the write control signal / read control signal caause the memory bus interface hardware to issue write command / read command on the memory bus. The processor wait in this process until the memory operation is completed and an WMFC response is received.

6. **How do you control instructions like branch, cause problems in a pipelined processor?**

Pipelined processor gives the best throughput for sequenced line instruction. In branch instruction, as it has to calculate the target address, whether the instruction jump from one memory location to other. In the mean time, before calculating the larger, the next sequence instructions are got into the pipelines, which are rolled back when target is calculated.

7. **What is the function of a TLB (translation look-aside buffer)?**

A small cache called the TLB is interporated into MMU, which consists of the page table entries that corresponding to the most recently accessed page.

8. An eight-way set-associative cache consists of a total of 256 blocks. The main memory, contains 8192 blocks, each consisting of 128 words.

(a) How many bits are there in the main memory address?

(b) How many bits are there in the TAG, SET and WORD fields?

The main memory contains of 256 blocks and each block consists of 128 words.

(a) Total words in MM = 8192 * 128 = 1048576.

(b) To address 32768 words we require (2^{20} = 1048576) 20 bits

9. Why are interrupt masks provided in any processor?

Interrupt mask enable the higher priority devices comes first and there for lower priority devices comes last. The interrupt enable bits as a bit vector is called as interrupt mask. Which enables / disables the devices according to the correct configuration of the mask.

10. How does bus arbitration typically work?

i. A bus master waiting to use the bus asserts by the bus request.

ii. A bus master cannot be the bus until it's request is granted.

iii. A bus master must signal to the arbitor at the end of the bus utilization.

PART B – (5×16=80 marks)

11. (i) Explain in detail the different types of instructions that are supported in a typical processor. (10) **Page No: 38**

(ii) Registers R1 and R2 of a computer contain the decimal values 1200 and 2400 respectively. What is the effective address of the memory operand in each of the following instructions?

(1) Load 20(R1), R5

(2) Add –(R2), R5

(3) Move #3000, R5

(4) Sub (R1)+, R5 (6)

Or

12. (a) (i) Explain in detail the principle of carry-look-ahead adder. Show how 16-bit CLAs can be constructed from 4-bit adders. (12)

Page No: 372

(ii) Perform the division on the following 5-bit unsigned integer using non-restoring division: 10101 / 00101. (4) **Page No: 390**

OR

(b) (i) Explain the working of a floating point adder/subtractor. (12)

Page No: 393

(ii) Multiply the following pair of signed 2's complement numbers using bit-pair recording of the multipliers : A = 010111, B = 101100. (4)

Page No: 384

13. (a) (i) Explain how pipelining helps to speed-up the processor. Discuss the hazards that have to be taken care of in a pipe-lined processor. (12)

Page No: 454

(ii) Give the sequence of control signals to be generated to fetch an instruction from memory in a single-bus organization. (4)

OR

(b) Explain in detail the working of a micro-programmed control unit. (16)

Page No: 429

14. (a) (i) Discuss the address translation mechanism and the different page replacement policies used in virtual memory system. (10)

Page No: 337

(ii) A byte addressable computer has a small data cache capable of holding eight 32-bit words. Each cache block contains 132-bit word. When a given program is executed, the processor reads data from the following sequence of hex addresses – 200, 204, 208, 20C, 2F4, 2F0, 200, 204, 218, 21C, 24C, 2F4. The pattern is repeated four times. Assuming that the cache is initially empty, show the contents of the cache at the end of each pass, and compute the hit rate for a direct mapped cache. (6)

OR

14 (b) (i) Discuss the various mapping schemes used in cache design.Comare the schemes in terms of cost and performance.(10)

Page No: 316

(ii) Consider a two –level cache with access times of 5 ns, and 8-0 ns respectively.If the hit rates are 95%and 75% respectively in the two caches,and the memory access time is 250ns,what is the average access time?

15 (a) (i) Explain the use of vectored interrupts in processors.Why is priority handling desired in interrupt controllers?How do the different priority schemes work ? (10) **Page No: 208**

(ii) Discuss the data transfer mechanism of the PCI bus.(6) **Page No: 261**

OR

(b) (i) Explain how data may be transferred from a hard disk to memory using DMA including arbitration for the bus.Assume a synchronous bus,and draw a timing diagram showing the data transfer.(10)

Page No: 234

(ii) Discuss the salient features of the USB operation(6) **Page No: 272**

CS 2254 OPERATING SYSTEMS

SYLLABUS

Unit I Processes and threads 9

Introduction to operating systems – review of computer organization – operating system structures – system calls – system programs – system structure – virtual machines. Processes: Process concept – Process scheduling – Operations on processes – Cooperating processes – Interprocess communication – Communication in client-server systems. Case study: IPC in Linux. Threads: Multi-threading models – Threading issues. Case Study: Pthreads library

Unit II Process Scheduling and Synchronization 10

CPU Scheduling: Scheduling criteria – Scheduling algorithms – Multiple-processor scheduling – Real time scheduling – Algorithm Evaluation. Case study: Process scheduling in Linux. Process Synchronization: The critical-section problem – Synchronization hardware – Semaphores – Classic problems of synchronization – critical regions – Monitors. Deadlock: System model – Deadlock characterization – Methods for handling deadlocks – Deadlock prevention – Deadlock avoidance – Deadlock detection – Recovery from deadlock.

Unit III Storage Management 9

Memory Management: Background – Swapping – Contiguous memory allocation – Paging – Segmentation – Segmentation with paging. Virtual Memory: Background – Demand paging – Process creation – Page replacement – Allocation of frames – Thrashing. Case Study: Memory management in Linux

Unit IV File Systems 9

File-System Interface: File concept – Access methods – Directory structure – File-system mounting – Protection. File-System Implementation : Directory implementation – Allocation methods – Free-space management – efficiency and performance – recovery – log-structured file systems. Case studies: File system in Linux – file system in Windows XP

Unit V I/O Systems 8

I/O Systems – I/O Hardware – Application I/O interface – kernel I/O subsystem – streams – performance. Mass-Storage Structure: Disk scheduling – Disk management – Swap-space management – RAID – disk attachment – stable storage – tertiary storage. Case study: I/O in Linux

TOTAL: 45

TEXT BOOK:

1. Silberschatz, Galvin, and Gagne, “Operating System Concepts”, Sixth Edition, Wiley India Pvt Ltd, 2003.

REFERENCES:

1. Andrew S. Tanenbaum, “Modern Operating Systems”, Second Edition, Pearson Education/PHI 2001.
2. Gary Nutt, “Operating Systems”, Third Edition, Pearson Education, 2004.
3. Harvey M. Deital, “Operating Systems”, Third Edition, Pearson Education, 2004.

UNIT 1 - INTRODUCTION

2 MARKS

1. What is an operating system?

Answer:

An operating system is a program that manages the computer hardware. it act as an intermediate between a users of a computer and the computer hardware. It controls and coordinates the use of the hardware among the various application programs for the various users.

2. What is the kernel?

Answer:

A more common definition is that the OS is the one program running at all times on the computer usually called the kernel, with all else being application programs.

3. What are batch systems?

Answer:

Batch systems are quite appropriate for executing large jobs that need little interaction. The user can submit jobs and return later for the results. It is not necessary to wait while the job is processed.

4. What is graceful degradation?

Answer:

In multiprocessor systems, failure of one processor will not halt the system, but only slow it down by sharing the work of failure system by other

systems. This ability to continue providing service is proportional to the surviving hardware is called graceful degradation.

5. Differentiate tightly coupled systems and loosely coupled systems?

Answer:

Loosely coupled systems:-

Each processor has its own local memory

Each processor can communicate with other all through communication lines

Tightly coupled systems:-

Common memory is shared by many processors

No need of any special communication lines

6. What is real time system?

Answer:

A real time system has well defined, fixed time constraints. Processing must be done within the defined constraints, or the system will fail. It is often used as a control device in a dedicated application.

7. What are privileged instructions?

Answer:

Some of the machine instructions that may cause harm to a system are designated as privileged instructions. The hardware allows the privileged instructions to be executed only in monitor mode.

8. What do you mean by system calls?

Answer:

System calls provide the interface between a process and the operating system. When a system call is executed, it is treated as by the hardware as software interrupt.

10. What is a process?

Answer:
A process is a program in execution. It is an active entity and it includes the process stack, containing temporary data and the data section contains global variables.

11. What is process control block?

Answer:
Each process is represented in the OS by a process control block. It contain many pieces of information associated with a specific process.

12. What is scheduler?

Answer:
A process migrates between the various scheduling queues through out its life time. The OS must select processes from these queues in some fashion. This selection process is carried out by a scheduler.

13. What are the use of job queues, ready queues and device queues?

Answer:
As a process enters a system they are put in to a job queue. This queues consist of all jobs in the system. The processes that are residing in main memory and are ready and waiting to execute are kept on a list called ready queue. The list of processes waiting for particular I/O devices kept in the device queue.

14. What is meant by context switch?

Answer:
Switching the CPU to another process requires saving the state of the old process and loading the saved state for the new process. This task is known as context switch.

15. What is independent process?

Answer:
A process is independent it cannot affect Or be affected by the other processes executing in the system. Any process does not share data with other process is a independent process.

16. What is co-operative process?

Answer:
A process is co-operating if it can affect or be affected by the other processes executing in the system. Any process that share data with other process is a co-operating process.

17. What is the benefits OS co-operating process?

Answer:
**Information sharing.

** Computation speeds up.

**Modularity.

**Convenience.

18. How can a user program disturb the normal operation of the system?

Answer:
**Issuing illegal I/O operation.

**By accessing memory locations with in the OS itself.

**Refusing to relinquish the CPU.

19. State the advantage of multiprocessor system?

Answer:
Increased throughput.

Economy of scale.

Increased reliability.

20. What is the use of inter process communication.

Answer:
Inter process communication provides a mechanism to allow the co-operating process to communicate with each other and synchronies their actions without sharing the same address space. It is provided a message passing system.

21. What is spooling?

Answer:
Spooling overlaps the I/O of one job with the computation of other jobs.

22. Classify Real time systems.

Answer:
Soft real time systems

Hard real time systems

23. Discuss difference between symmetric and asymmetric multiprocessing

Answer:

Symmetric multiprocessing (SMP), in which each processor runs an identical copy of the operating system and these copies, communicate with one another as needed.

Asymmetric multiprocessing, in which each processor is assigned a specific task. The master processor controls the system; the other processor looks the master.

24. What are the three main purposes of an operating system?

Answer:

_ To provide an environment for a computer user to execute programs on computer hardware in a convenient and efficient manner.

_ To allocate the separate resources of the computer as needed to solve the problem given. The allocation process should be as fair and efficient as possible.

_ As a control program it serves two major functions: (1) supervision of the execution of user programs to prevent errors and improper use of the computer, and (2) management of the operation and control of I/O devices.

25. List the four steps that are necessary to run a program on a completely dedicated machine.

Answer:

a. Reserve machine time.

b. Manually load program into memory.

c. Load starting address and begin execution.

d. Monitor and control execution of program from console.

26. What is the main advantage of multiprogramming?

Answer: Multiprogramming makes efficient use of the CPU by overlapping the demands for the CPU and its I/O devices from various users. It attempts

to increase CPU utilization by always having something for the CPU to execute.

27. What are the main differences between operating systems for mainframe computers and personal computers?

Answer: The design goals of operating systems for those machines are quite different. PCs are inexpensive, so wasted resources like CPU cycles are inconsequential. Resources are wasted to improve usability and increase software user interface functionality. Mainframes are the opposite, so resource use is maximized, at the expensive of ease of use.

28. In a multiprogramming and time-sharing environment, several users share the system simultaneously.

This situation can result in various security problems.

a. What are two such problems?

b. Can we ensure the same degree of security in a time-shared machine as we have in a dedicated machine? Explain your answer.

Answer:

a. Stealing or copying one's programs or data; using system resources (CPU, memory, disk space, peripherals) without proper accounting.

b. Probably not, since any protection scheme devised by humans can inevitably be broken by a human, and the more complex the scheme, the more difficult it is to feel confident of its correct implementation.

29. Define the essential properties of the following types of operating systems:

a. Batch

b. Interactive

c. Time sharing

d. Real time

e. Network

f. Distributed

Answer:

a. *Batch*. Jobs with similar needs are batched together and run through the computer as a group by an operator or automatic job sequencer. Performance is increased by attempting to keep CPU and I/O devices busy at all times through buffering, off-line operation, spooling, and multiprogramming. Batch is good for executing large jobs that need little interaction; it can be submitted and picked up later.

b. *Interactive*. This system is composed of many short transactions where the results of the next transaction may be unpredictable. Response time needs to be short (seconds) since the user submits and waits for the result.

c. *Time sharing*. This systems uses CPU scheduling and multiprogramming to provide economical interactive use of a system. The CPU switches rapidly from one user to another. Instead of having a job defined by spooled card images, each program reads its next control card from the terminal, and output is normally printed immediately to the screen.

d. *Real time*. Often used in a dedicated application, this system reads information from sensors and must respond within a fixed amount of time to ensure correct performance.

e. *Network.*

f. *Distributed.* This system distributes computation among several physical processors. The processors do not share memory or a clock. Instead, each processor has its own local memory. They communicate with each other through various communication lines, such as a high-speed bus or telephone line.

30. We have stressed the need for an operating system to make efficient use of the computing hardware. When is it appropriate for the operating system to forsake this principle and to "waste" resources? Why is such a system not really wasteful?

Answer: Single-user systems should maximize use of the system for the user. A GUI might "waste" CPU cycles, but it optimizes the user's interaction with the system.

31. Under what circumstances would a user be better off using a time-sharing system, rather than a personal computer or single-user workstation?

Answer: When there are few other users, the task is large, and the hardware is fast, timesharing makes sense. The full power of the system can be brought to bear on the user's problem. The problem can be solved faster than on a personal computer. Another case occurs when lots of other users need resources at the same time.

A personal computer is best when the job is small enough to be executed reasonably on it and when performance is sufficient to execute the program to the user's satisfaction.

32. Describe the differences between symmetric and asymmetric multiprocessing. What are three advantages and one disadvantage of multiprocessor systems?

Answer: Symmetric multiprocessing treats all processors as equals and I/O can be processed on any CPU. Asymmetric multiprocessing has one master CPU and the remainder CPUs are slaves. The master distributes tasks among the slaves, and I/O is usually done by the master only. Multiprocessors can save money by not duplicating power supplies, housings, and peripherals. They can execute programs more quickly and can have increased reliability.

They are also more complex in both hardware and software than uniprocessor systems.

33. What is the main difficulty that a programmer must overcome in writing an operating system for a real-time environment?

Answer: The main difficulty is keeping the operating system within the fixed time constraints of a real-time system. If the system does not complete a task in a certain time frame, it may cause a breakdown of the entire system it is running. Therefore when writing an operating system for a real-time system, the writer must be sure that his scheduling schemes don't allow response time to exceed the time constraint.

34. What are the five major activities of an operating system in regard to process management?

Answer:

_ The creation and deletion of both user and system processes

_ The suspension and resumption of processes

_ The provision of mechanisms for process synchronization

_ The provision of mechanisms for process communication

_ The provision of mechanisms for deadlock handling

35. What are the three major activities of an operating system in regard to memory management?

Answer:

_ Keep track of which parts of memory are currently being used and by whom.

_ Decide which processes are to be loaded into memory when memory space becomes available.

_ Allocate and deallocate memory space as needed.

36. What are the three major activities of an operating system in regard to secondary-storage management?

Answer:

_ Free-space management.

_ Storage allocation.

_ Disk scheduling.

37. What are the five major activities of an operating system in regard to file management?

Answer:

_ The creation and deletion of files

_ The creation and deletion of directories

_ The support of primitives for manipulating files and directories

_ The mapping of files onto secondary storage

_ The backup of files on stable (nonvolatile) storage media

38. What is the purpose of the command interpreter? Why is it usually separate from the kernel?

Answer: It reads commands from the user or from a file of commands and executes them, usually by turning them into one or more system calls. It is usually not part of the kernel since the command interpreter is subject to changes.

39. What is the purpose of system calls?

Answer: System calls allow user-level processes to request services of the operating system.

40. What is the purpose of system programs?

Answer: System programs can be thought of as bundles of useful system calls. They provide basic functionality to users and so users do not need to write their own programs to solve common problems.

41. What is the main advantage of the layered approach to system design?

Answer: As in all cases of modular design, designing an operating system in a modular way has several advantages. The system is easier to debug and modify because changes affect only limited sections of the system rather than touching all sections of the operating system. Information is kept only where it is needed and is accessible only within a defined and restricted area, so any bugs affecting that data must be limited to a specific module or layer.

42. What are the main advantages of the microkernel approach to system design?

Answer: Benefits typically include the following

(a) adding a new service does not require modifying the kernel,

(b) it is more secure as more operations are done in user mode than in kernel mode, and

(c) a simpler kernel design and functionality typically results in a more reliable operating system.

16 MARKS

1. List five services provided by an operating system. Explain how each provides convenience to the users. Explain also in which cases it would be impossible for user-level programs to provide these services.

Answer:

_ *Program execution*. The operating system loads the contents (or sections) of a file into memory and begins its execution. A user-level program could not be trusted to properly allocate CPU time.

_ *I/O operations*. Disks, tapes, serial lines, and other devices must be communicated with at a very low level. The user need only specify the device and the operation to perform on it, while the system converts that request into device- or controller-specific commands. User-level programs cannot be trusted to only access devices they should have access to and to only access them when they are otherwise unused.

_ *File-system manipulation*. There are many details in file creation, deletion, allocation, and naming that user should not have to perform. Blocks of disk space are used by files and must be tracked. Deleting a file requires removing the name file information and freeing the allocated blocks. Protections must also be checked to assure proper file access. User programs could neither ensure adherence to protection methods nor be trusted to allocate only free blocks and deallocate blocks on file deletion.

_ *Communications.* Message passing between systems requires messages be turned into packets of information, sent to the network controller, transmitted across a communications medium, and reassembled by the destination system. Packet ordering and data correction must take place. Again, user programs might not coordinate access to the network device, or they might receive packets destined for other processes.

_ *Error detection*. Error detection occurs at both the hardware and software levels. At the hardware level, all data transfers must be inspected to ensure that data have not been corrupted in transit. All data on media must be checked to be sure they have not changed since they were written to the media. At the software level, media must be checked for data consistency; for instance, do the numbers of allocated and unallocated blocks of storage match the total number on the device. There, errors are frequently process-independent (for instance, the corruption of data on a disk), so there must be

a global program (the operating system) that handles all types of errors. Also, by having errors processed by the operating system, processes need not contain code to catch and correct all the errors possible on a system.

2. Describe the differences among short-term, medium-term, and long-term scheduling.

Answer:

_ *Short-term (CPU scheduler)*—selects from jobs in memory those jobs that are ready to execute and allocates the CPU to them.

_ *Medium-term*—used especially with time-sharing systems as an intermediate scheduling level. A swapping scheme is implemented to remove partially run programs from memory and reinstate them later to continue where they left off.

_ *Long-term (job scheduler)*—determines which jobs are brought into memory for processing.

3. Explain the various types of computer systems.

Answer:

Mainframe systems

- Large Number of CPU with Greatest Processing Power:
- Huge Memory Capacity:
- Increased Performance by Sharing workload:
- Centralized Computing:
- Ability to Run in Multiple Operating System:
- Supports Time Sharing Ability:
- Supports Sophisticated Operating system:
- Reliability:
- Availability:

- Serviceability:
- Supports Maximum I/O connectivity
  Have capability of providing Maximum I/O bandwidth
  Have the greatest ability of producing fault tolerant computing.
  Capacity to manage Large Users

Desktop systems

- *Personal computers* – computer system dedicated to a single user.
- I/O devices – keyboards, mice, display screens, small printers.
- User convenience and responsiveness.
- Can adopt technology developed for larger operating system' often individuals have sole use of computer and do not need advanced CPU utilization of protection features.
- May run several different types of operating systems (Windows, MacOS, UNIX, Linux)

Multiprocessor systems

- Multiprocessor systems with more than on CPU in close communication.
- *Tightly coupled system* – processors share memory and a clock; communication usually takes place through the shared memory.
- Advantages of parallel system:
  - Increased *throughput*
  - Economical
  - Increased reliability
    - graceful degradation
    - fail-soft systems

- *Symmetric multiprocessing (SMP)*
    - Each processor runs and identical copy of the operating system.
    - Many processes can run at once without performance deterioration.
    - Most modern operating systems support SMP
- *Asymmetric multiprocessing*
    - Each processor is assigned a specific task; master processor schedules and allocated work to slave processors.
    - More common in extremely large systems

Distributed systems

- Distribute the computation among several physical processors.
- *Loosely coupled system* – each processor has its own local memory; processors communicate with one another through various communications lines, such as high-speed buses or telephone lines.
- Advantages of distributed systems.
    - Resources Sharing
    - Computation speed up – load sharing
    - Reliability
    - Communications

Clustered systems

- Clustering allows two or more systems to share storage.
- Provides high reliability.
- *Asymmetric clustering*: one server runs the application while other servers standby.
- *Symmetric clustering*: all N hosts are running the application.

Real-time systems

- Often used as a control device in a dedicated application such as controlling scientific experiments, medical imaging systems, industrial control systems, and some display systems.
- Well-defined fixed-time constraints.
- Real-Time systems may be either *hard* or *soft* real-time.
- Hard real-time:
    - Secondary storage limited or absent, data stored in short term memory, or read-only memory (ROM)
    - Conflicts with time-sharing systems, not supported by general-purpose operating systems.
- Soft real-time
    - Limited utility in industrial control of robotics
    - Useful in applications (multimedia, virtual reality) requiring advanced operating-system features.

Handheld systems

- Personal Digital Assistants (PDAs)
- Cellular telephones
- Issues:
    - Limited memory
    - Slow processors
    - Small display screens.

Time-sharing Systems

- Time sharing (or multitasking) is a logical extension of multiprogramming. The

- CPU executes multiple jobs switching among them, but the switches occurs so frequently that the users can interact with each program while it is running.
- An interactive (or hands-on) computer system provides direct communication between the user and the system.
- A time-shared operating system allows many users to share the computer simultaneously. As the system switches rapidly from one user to the next, each user is given an imprison that the entire system is dedicated to one user.
- Time-shared operating system uses CPU scheduling and multiprogramming to provide each user with a small portion of a time-shared computer. A program loaded into memory and executing is commonly referred to as a process.
- Time-sharing operating systems are even more complex than multiprogrammed operating system. To obtain a reasonable response time, jobs may have to be swapped in and out of main memory to the disk. A common method for achieving this goal is virtual memory. It is a technique that allows the execution of a job that may have not be completely in memory. The main advantage of the virtual-memory scheme is that programs can be larger than physical memory.
- Time-sharing systems must also provide a file system that resides on a collection of disks. Time-sharing system

provides a mechanism for concurrent execution. To ensure orderly execution, the system must provide mechanism for job synchronization and communication.

4. Explain how protection is provided for the hardware resources by the operating system.

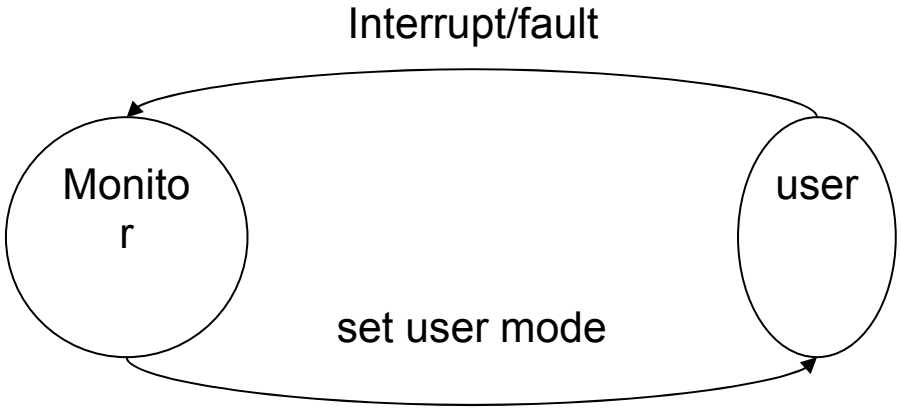
Answer:

Dual mode operation

- Sharing system resources requires operating system to ensure that an incorrect program cannot cause other programs to execute incorrectly.
- Provide hardware support to differentiate between at least two modes of operations.

1. *User mode* – execution done on behalf of a user.
2. *Monitor mode* (also *kernel mode* or *system mode*) – execution done on behalf of operating system.

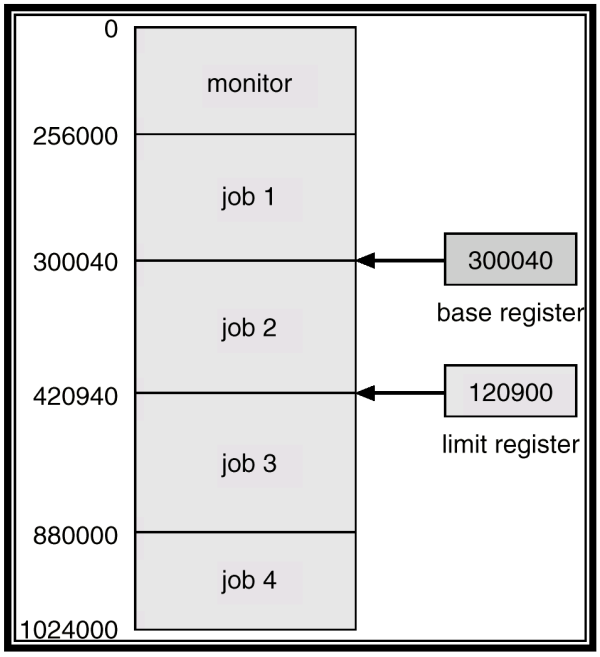
- *Mode bit* added to computer hardware to indicate the current mode: monitor (0) or user (1).
- When an interrupt or fault occurs hardware switches to monitor mode.

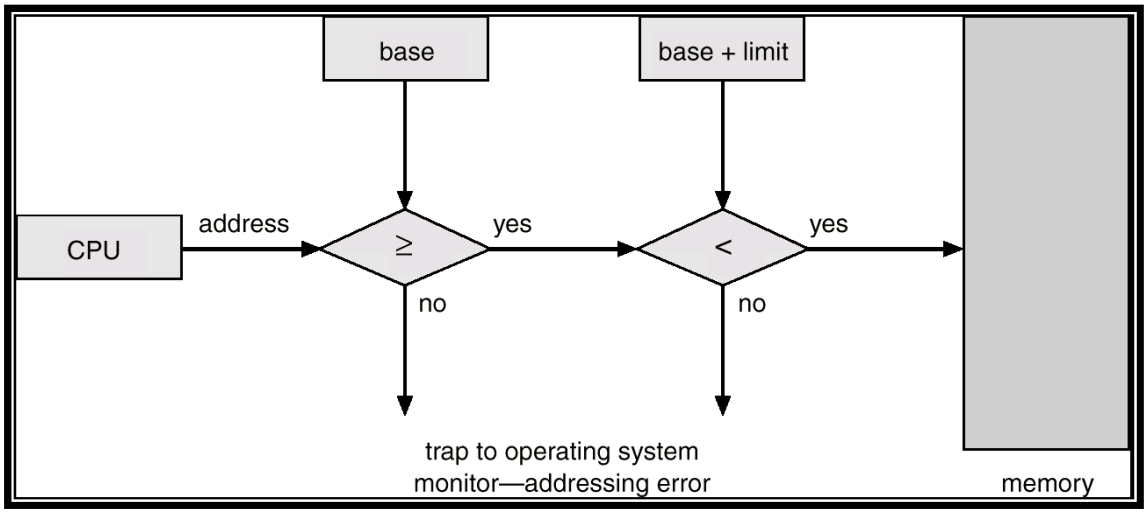


I/O protection with diagram

- All I/O instructions are privileged instructions.
- Must ensure that a user program could never gain control of the computer in monitor mode (I.e., a user program that, as part of its execution, stores a new address in the interrupt vector).

Memory protection with diagram

- Must provide memory protection at least for the interrupt vector and the interrupt service routines.
- In order to have memory protection, add two registers that determine the range of legal addresses a program may access:
  - Base register – holds the smallest legal physical memory address.
  - Limit register – contains the size of the range
- Memory outside the defined range is protected.
- 



CPU protection

- *Timer* – interrupts computer after specified period to ensure operating system maintains control.
  - Timer is decremented every clock tick.
  - When timer reaches the value 0, an interrupt occurs.
- Timer commonly used to implement time sharing.
- Time also used to compute the current time.
- Load-timer is a privileged instruction.

5. What are the system components of an operating system and explain them?

Answer: Explain all the topics in detail

Process management

Main-memory management

File management

I/O management

Secondary storage management

Networking

Protection system

Command-interpreter system

6. What are the various process scheduling concepts?

Answer: Explain all the topics in detail

Scheduling queues with diagram

Queuing diagram

Schedulers

Context switch with diagram

7. Explain about interprocess communication. (AU-nov/dec 2006)

Answer:

The cooperating processes communicate with each other via an interprocess communication facility. IPC provides a mechanism to allow processes to communicate and to synchronize their actions without sharing the same address space. It is particularly useful in a distributed environment.

Message passing system:-

The function of message system is to allow processes to communicate with one another without the need to resort (option) to shared data. Communication among the user processes is accomplished through the passing of messages. An IPC facility provides at least two operations: send and receive.

If processes P and Q want to communicate, they must send messages to and receive messages from each other; a communication link must exist between them.

Methods for logically implementing links

o Direct or indirect communication.

o Symmetric or asymmetric communication.

o Automatic or explicit buffering.

o Sent by copy or send by reference.

o Fixed-sized or variable-sized messages.

Naming

To refer the processes involved in communication.

Direct communication

With direct communication each process that wants to communicate must explicitly name the recipient or sender of the communication. The send and receive primitives are

o Send (P,message) – Send a message to process P.

o Receive (Q,message) – Receive a message from process Q.

A communication link has the following properties.

._ A link is established automatically between every pair of processes that want to communicate.

_ A link is associated with exactly two processes.

_ Exactly one link exists between each pair of processes.

Another scheme in communication employs asymmetry in addressing. Only the sender names the recipient; the recipient is not required to name the sender. The send are receive primitives in this scheme are

o Send (P,message) – Send a message to process P.

o Receive (id,message) – Receive a message from any process; the variable id is the name of the processes with which the communication has taken place.

Indirect communication

With indirect communication, the messages are sent to and received from mailboxes or ports. A mailbox can be viewed abstractly as an object into which messages can be placed by processes and from which messages can be removed. Each mailbox has a unique identification. Two processes can communicate only if they share a mailbox. The primitives are

o Send (A, message) – Send a message to mailbox A.

o Receive (A, message) – Receive a message from mailbox A.

A communication link has the following properties.

._ A link is established between a pair of processes only if both members of the pair have a shared mailbox.

_ A link may be associated with more than two processes.

_ Each link corresponding to one mailbox.

A mailbox may be owned either by processes or by the operating system. If the mailbox is owned by the process then we distinguish between the owner (receive message) and the user (send message).

Mailbox owned by the operating system is independent and is not attached to any particular process. The OS allows the process to do the following

o Create a new mailbox

o Send and receive messages through the mailbox.

o Delete a mailbox.

The process that creates a new mailbox is that mailbox's owner by default.

Synchronization

In communication between processes messages passed may be blocking or nonblocking – also known as synchronous and asynchronous.

o Blocking send : The sending process is blocked until the message is received.

o Nonblocking send: The sending process sends the message and resumes operation.

o Blocking receive: The receiver blocks until a message is available.

o Nonblocking receive: The receiver retrieves either a valid message or a null.

Buffering

Messages exchanged by communication processes reside in a temporary queue. Such a queue can be implemented in three ways.

- Zero capacity: The queue length is 0. In this case, the sender must block until the recipient receives the message.
- Bounded capacity: The queue has finite length n, at most n message can reside in it.
- If the link is full, the sender must block until space is available in the queue.
- Unbounded capacity: The queue has potentially infinite length. The sender never blocks.

8. List and discuss the various services provided by the operating system. Nov/dec 2007

Answer:

- Program execution – system capability to load a program into memory and to run it.
- I/O operations – since user programs cannot execute I/O operations directly, the operating system must provide some means to perform I/O.
- File-system manipulation – program capability to read, write, create, and delete files.

- Communications – exchange of information between processes executing either on the same computer or on different systems tied together by a network.
- Error detection – ensure correct computing by detecting errors in the CPU and memory hardware, in I/O devices, or in user programs.

Additional functions exist not for helping the user, but rather for ensuring efficient system operations.

- Resource allocation – allocating resources to multiple users or multiple jobs running at the same time.
- Accounting – keep track of and record which users use how much and what kinds of computer resources for account billing or for accumulating usage statistics.
- Protection – ensuring that all access to system resources is controlled.

9. What are the operations of processes?

Answer:

Process creation

A process may create several new processes. The creating process is called a parent process, where as the new process is called the children processes. When a processes creates a sub processes, the parent may have to partition its resources among its children.

When a process creates new processes, two possibilities exist in terms of execution.

1. The parent continues to execute concurrently with its children.
2. The parent waits until some or all of its children have terminated.

In regarding the address space

1. The child process is a duplicate of the parent process.

2. The child process has a program loaded into it.

In UNIX, each process is identified by its process identifier, which is a unique integer. A new process is created by the fork system call. The new process consists of a copy of the address space of the original process. The execlp system call is used to replace the processes memory space with a new program.

Process termination

A process terminates when it finishes executing its final statement and asks the operating system to delete it by using the exit system call. At that time the process may return data to its parent processes. All the resources are deallocated by the operating system.

A parent may terminate the execution of one of its children's for a variety of reasons.

._ The child has exceeded its usage of some of the resources that it has been allocated.

._ The task assigned to the child is no longer required.

._ The parent is exiting. On such systems, if processes terminates, then all its children must also be terminated. This phenomenon, referred to as cascading termination.

In UNIX we can terminate processes by using exit system call.

UNIT 2 – THREADS, CPU SCHEDULING, PROCESS SYNCHRONIZATION

2 MARKS

1. What is a thread?

Answer:

A thread otherwise called a lightweight process (LWP) is a basic unit of CPU utilization, it comprises of a thread id, a program counter, a register set and a stack. It shares with other threads belonging to the same process its code section, data section, and operating system resources such as open files and signals.

2. What are the benefits of multithreaded programming?

Answer:

The benefits of multithreaded programming can be broken down into four major categories:

• Responsiveness

• Resource sharing

• Economy

• Utilization of multiprocessor architectures

3. Compare user threads and kernel threads.

Answer:

User threads:-

User threads are supported above the kernel and are implemented by a thread library at the user level. Thread creation & scheduling are done in the user space, without kernel intervention. Therefore they are fast to create and manage blocking system call will cause the entire process to block

Kernel threads:-

Kernel threads are supported directly by the operating system .Thread creation, scheduling and management are done by the operating system. Therefore they are slower to create & manage compared to user threads. If the thread performs a blocking system call, the kernel can schedule another thread in the application for execution

4. What is the use of fork and exec system calls?

Answer:

Fork is a system call by which a new process is created. Exec is also a system call, which is used after a fork by one of the two processes to place the process memory space with a new program.

5. Define thread cancellation & target thread.

Answer:

The thread cancellation is the task of terminating a thread before it has completed. A thread that is to be cancelled is often referred to as the target thread. For example, if multiple threads are concurrently searching through a database and one thread returns the result, the remaining threads might be cancelled.

6. What are the different ways in which a thread can be cancelled?

Answer:

Cancellation of a target thread may occur in two different scenarios:

• Asynchronous cancellation: One thread immediately terminates the target thread is called asynchronous cancellation.

• Deferred cancellation: The target thread can periodically check if it should terminate, allowing the target thread an opportunity to terminate itself in an orderly fashion.

7. Define CPU scheduling.

Answer:

CPU scheduling is the process of switching the CPU among various processes. CPU scheduling is the basis of multiprogrammed operating systems. By switching the CPU among processes, the operating system can make the computer more productive.

8. What is preemptive and nonpreemptive scheduling?

Answer:

Under nonpreemptive scheduling once the CPU has been allocated to a process, the process keeps the CPU until it releases the CPU either by terminating or switching to the waiting state. Preemptive scheduling can preempt a process which is utilizing the CPU in between its execution and give the CPU to another process.

9. What is a Dispatcher?

Answer:

The dispatcher is the module that gives control of the CPU to the process selected by the short- term scheduler. This function involves:

• Switching context

• Switching to user mode

• Jumping to the proper location in the user program to restart that program.

10. What is dispatch latency?

Answer:

The time taken by the dispatcher to stop one process and start another running is known as dispatch latency.

11. What are the various scheduling criteria for CPU scheduling?

Answer:

The various scheduling criteria are

• CPU utilization

• Throughput
• Turnaround time
• Waiting time
• Response time

12. Define throughput?

Answer:

Throughput in CPU scheduling is the number of processes that are completed per unit time. For long processes, this rate may be one process per hour; for short transactions, throughput might be 10 processes per second.

13. What is turnaround time?

Answer:

Turnaround time is the interval from the time of submission to the time of completion of a process. It is the sum of the periods spent waiting to get into memory, waiting in the ready queue, executing on the CPU, and doing I/O.

14. Define race condition.

Answer:

When several process access and manipulate same data concurrently, then the outcome of the execution depends on particular order in which the access takes place is called race condition. To avoid race condition, only one process at a time can manipulate the shared variable.

15. What is critical section problem?

Answer:

Consider a system consists of 'n' processes. Each process has segment of code called a critical section, in which the process may be changing common variables, updating a table, writing a file. When one process is executing in its critical section, no other process can allowed executing in its critical section.

16. What are the requirements that a solution to the critical section problem must satisfy?

Answer:

The three requirements are

• Mutual exclusion

• Progress

• Bounded waiting

17. Define entry section and exit section.

Answer:

The critical section problem is to design a protocol that the processes can use to cooperate. Each process must request permission to enter its critical section. The section of the code implementing this request is the entry section. The critical section is followed by an exit section. The remaining code is the remainder section.

18. Give two hardware instructions and their definitions which can be used for implementing mutual exclusion.

Answer:

• TestAndSet

```
boolean TestAndSet (boolean &target)
{
boolean rv = target;
target = true;
return rv;
}
```

• Swap

```
void Swap (boolean &a, boolean &b)
{
```

```
boolean temp = a;
a = b;
b = temp;
}
```

19. What is a semaphore?

Answer:

A semaphore 'S' is a synchronization tool which is an integer value that, apart from initialization, is accessed only through two standard atomic operations; wait and signal .Semaphores can be used to deal with the n-process critical section problem. It can be also used to solve various Synchronization problems.

20. Define busy waiting and spinlock.

Answer:

When a process is in its critical section, any other process that tries to enter its critical section must loop continuously in the entry code. This is called as busy waiting and this type of semaphore is also called a spinlock, because the process while waiting for the lock.

21. Provide two programming examples of multithreading giving improved performance over a single-threaded solution.

Answer:

(1) A Web server that services each request in a separate thread.

(2) A parallelized application such as matrix multiplication where different parts of the matrix may be worked on in parallel.

(3) An interactive GUI program such as a debugger where a thread is used to monitor user input, another thread represents the running application, and a third thread monitors performance.

22. What are two differences between user-level threads and kernel-level threads? Under what circumstances is one type better than the other?

Answer:

(1) User-level threads are unknown by the kernel, whereas the kernel is aware of kernel threads.

(2) User threads are scheduled by the thread library and the kernel schedules kernel threads.

(3) Kernel threads need not be associated with a process whereas every user thread belongs to a process.

23. Define the difference between preemptive and nonpreemptive scheduling. State why strict nonpreemptive scheduling is unlikely to be used in a computer center.

Answer: Preemptive scheduling allows a process to be interrupted in the midst of its execution, taking the CPU away and allocating it to another process. Nonpreemptive scheduling ensures that a process relinquishes control of the CPU only when it finishes with its current CPU burst.

16 MARKS

1. Consider the following set of processes, with the length of the CPU-burst time given in milliseconds:

Process	Burst Time	Priority
***P*1**	**10**	**3**
***P*2**	**1**	**1**
***P*3**	**2**	**3**
***P*4**	**1**	**4**
***P*5**	**5**	**2**

The processes are assumed to have arrived in the order *P*1, *P*2, *P*3, *P*4, *P*5, all at time 0.

a. Draw four Gantt charts illustrating the execution of these processes using FCFS, SJF, a nonpreemptive priority (a smaller priority number implies a higher priority), and RR (quantum = 1) scheduling.

b. What is the turnaround time of each process for each of the scheduling algorithms in part a?

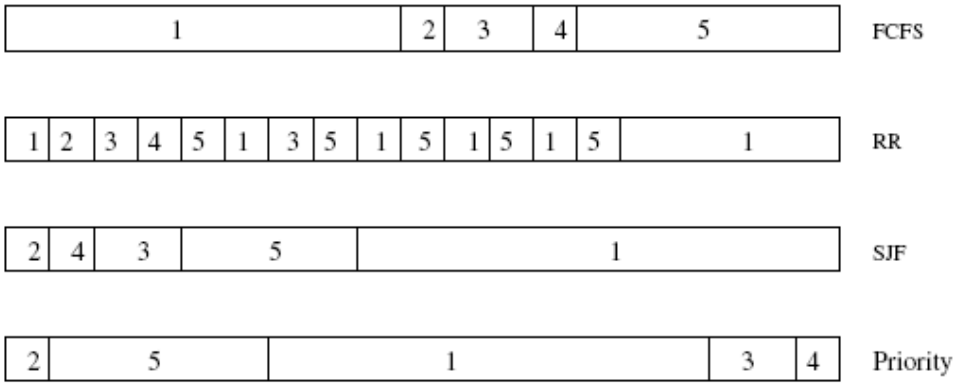
c. What is the waiting time of each process for each of the scheduling algorithms in part a?

d. Which of the schedules in part a results in the minimal average waiting time (over all processes)?

Answer:

Answer:

a. The four Gantt charts are



b. Turnaround time

	FCFS	RR	SJF	Priority
P_1	10	19	19	16
P_2	11	2	1	1
P_3	13	7	4	18
P_4	14	4	2	19
P_5	19	14	9	6

c. Waiting time (turnaround time minus burst time)

	FCFS	RR	SJF	Priority
P_1	0	9	9	6
P_2	10	1	0	0
P_3	11	5	2	16
P_4	13	3	1	18
P_5	14	9	4	1

d. Shortest Job First

2. Suppose that the following processes arrive for execution at the times indicated. Each process will run the listed amount of time. In answering the questions, use nonpreemptive scheduling and base all decisions on the information you have at the time the decision must be made.

Process	**Arrival Time**	**Burst Time**
***P*1**	**0.0**	**8**
***P*2**	**0.4**	**4**

***P*3 1.0 1**

a. What is the average turnaround time for these processes with the FCFS scheduling algorithm?

b. What is the average turnaround time for these processes with the SJF scheduling algorithm?

c. The SJF algorithm is supposed to improve performance, but notice that we chose to run process *P*1 at time 0 because we did not know that two shorter processes would arrive soon. Compute what the average turnaround time will be if the CPU is left idle for the first 1 unit and then SJF scheduling is used. Remember that processes *P*1 and *P*2 are waiting during this idle time, so their waiting time may increase. This algorithm could be known as future-knowledge scheduling.

Answer:

a. 10.53

b. 9.53

c. 6.86

Remember that turnaround time is finishing time minus arrival time, so you have to subtract the arrival times to compute the turnaround times. FCFS is 11 if you forget to subtract arrival time.

3. What are the multithreading models?

Answer:

There are three common types of threading implementations.

Many-to-One model

The many-to-one model maps many user-level threads to one kernel thread. Thread management is done in user space. One thread can access the kernel at a time. Green threads – a thread library available for Solaris 2.

One-to-One model

It maps each user thread to a kernel thread. It provides more concurrency than the many-to-one model. It allows multiple threads to run in parallel on multiprocessors.

Drawback is creating a user thread requires creating the corresponding kernel thread.

Windows NT, Windows 2000, and OS/2 implement the one-to-one model.

Many-to-Many model

It multiplexes many user-level threads to a smaller or equal number of kernel threads.

It allows the developer to create as many user threads as possible.

The shortcomings of this model are

1. Developers can create as many user threads as necessary, and the corresponding kernel threads can run in parallel on a multiprocessor.

2. When a thread performs a blocking system call, the kernel can schedule another thread for execution.

Solaris 2, IRIX, HP-UX, and Tru64 UNIX support this model.

4. Explain about threading issues?

Answer:

The fork and exec system calls

In a multithreaded program of some UNIX systems have chosen to have two versions of fork, one that duplicates all threads and another that duplicates only the thread that invoked the fork system call. If a thread invokes the exec system call, the program specified in the parameter to exec will replace the entire process.

Cancellation

Thread cancellation is the task of terminating a thread before it has completed. A thread that is to be cancelled is often referred to as the target thread. Cancellation of a target thread may occur in two scenarios.

1. Asynchronous cancellation: One thread immediately terminates the target thread.
2. Deferred cancellation: The target thread can periodically check if it should terminate.

Signal handling

A signal is used in UNIX systems to notify a process that a particular event has occurred.

1. A signal is generated by the occurrence of a particular event.
2. A generated signal is delivered to a process.
3. Once delivered, the signal must be handled.

Every signal may be handled by one of two possible handlers

1. A default signal handler.
2. A user-defined signal handler.

Every signal has a default signal handler that is run by the kernel when handling the signal. This default action may be overridden by user-defined signal handler function.

Delivering signals is more complicated in multithreaded programs, as a process may have several threads. In general the following options exist

1. Deliver the signal to the thread to which the signal applies.
2. Deliver the signal to every thread in the process.
3. Deliver the signal to certain threads in the process.
4. Assign a specific thread to receive all signals for the process.

Solaris 2 implements the fourth option. Although Windows 2000 does not explicitly provide support for signals, they can be emulated using asynchronous procedure calls

(APCs). The APC facility allows a user thread to specify a function that is to be called when the user thread receives notification of a particular event.

Thread pools

Creating a separate thread is superior to create a separate process. *Multithreaded server has potential problems.*

a) The amount of time required to create the thread prior to serving the request.

b) If we allow all concurrent requests to be serviced in a new thread, we have not placed a bound on the number of threads concurrently active in the system.

Unlimited threads could exhaust system resources, such as CPU time or memory. One solution to this issue is to use thread pools.

The benefits of thread pools are

1. It is usually faster to service a request with an existing thread than waiting to create a thread.

2. A thread pool limits the number of threads that exists at any one point.

Thread-specific data

Threads belonging to a process share the data of the process. Indeed, this sharing of data provides one of the benefits of multithreaded programming. However, each thread might need its own copy of certain data in some circumstances. We will call such data thread-specific data.

5. Briefly discuss on realtime scheduling?

Answer:

It is divided into two types.

Hard real-time systems are required to complete a critical task within a guaranteed amount of time. The scheduler then either admits the process, guaranteeing that the process will complete on time, or rejects the request as impossible.

This is known as resource reservation. Therefore, hard real-time systems are composed of special-purpose software running on hardware dedicated to their critical process.

Software real-time computing is less restrictive. It requires that critical processes receive priority over less fortune ones.

There are several ways to achieve preemptible to keep dispatch latency low. One is to insert preemption points in long-duration system calls that check to see whether a high priority process needs to run. Another method for dealing with preemption is to make the entire kernel preemptible.

In real-time scheduling, the high-priority process would be waiting for a lower priority one to finish. This situation is known as priority inversion. A chain of processes could all be accessing resources that the high-process needs. This problem can be solved vial the priority-inheritance protocol, in which all these processes inherit the high priority until they are done with the resource in question.

The conflict phase of dispatch latency has two components

1. Preemption of any process running in the kernel.

2. Release by low-priority processes resources needed by the high-priority process.

6. Explain multilevel feedback queue in detail

Answer:

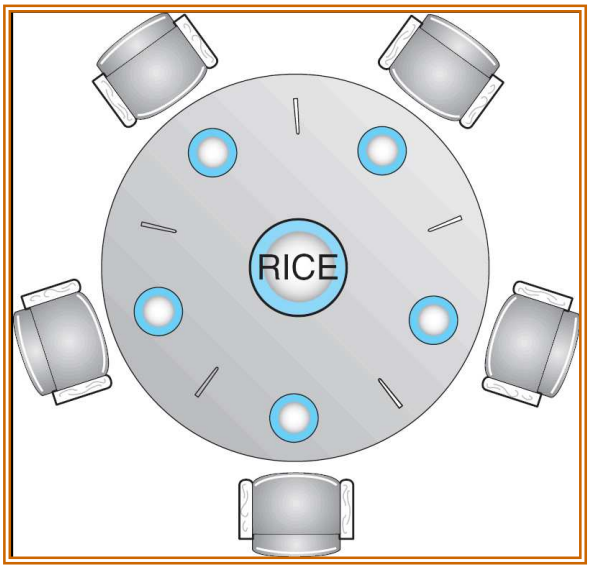
- A process can move between the various queues; aging can be implemented this way
- Multilevel-feedback-queue scheduler defined by the following parameters:
  - number of queues
  - scheduling algorithms for each queue
  - method used to determine when to upgrade a process
  - method used to determine when to demote a process
  - method used to determine which queue a process will enter when that process needs service

EXAMPLE:

- Three queues:
  - $Q0$ – RR with time quantum 8 milliseconds
  - $Q1$ – RR time quantum 16 milliseconds
  - $Q2$ – FCFS
- Scheduling
  - A new job enters queue *Q0* which is served FCFS. When it gains CPU, job receives 8 milliseconds. If it does not finish in 8 milliseconds, job is moved to queue $Q1$.
  - At $Q1$ job is again served FCFS and receives 16 additional milliseconds. If it still does not complete, it is preempted and moved to queue $Q2$.

7. State the dining philosopher's problem and show how to allocate the several resources among several processors in a deadlock and starvation free manner.

Answer: Also refer book for theory



- goal: to allocate several resources among several processes in a deadlock- and starvation-free manner
- Shared data
- Bowl of rice (data set)
- Semaphore chopstick [5] initialized to 1

- allow at most four philosophers to be sitting simultaneously at the table
    - a spare resource
- allow a philosopher to pick up chopsticks only if both are available, and pick up them simultaneously

- use a asymmetric solution: an odd philosopher picks up first the left chopstick and then the right chopstick, whereas an even one picks up first the right and then the left
- a deadlock-free solution does not eliminate the possibility of starvation
- The structure of Philosopher *i*:

```
while (true)  {
        wait ( chopstick[i] );
        wait ( chopstick[ (i + 1) % 5] );

             //  eat

        signal ( chopstick[i] );
        signal (chopstick[ (i + 1) % 5] );

             //  think

}
```

Solution to DINING philosopher problem

```
monitor DP
  {
      enum { THINKING; HUNGRY, EATING) state [5] ;
      condition self [5];

      void pickup (int i) {
```

```
            state[i] = HUNGRY;
            test(i);
            if (state[i] != EATING) self [i].wait;
        }

        void test (int i) {
            if ( (state[(i + 4) % 5] != EATING) &&
                (state[i] == HUNGRY) &&
                (state[(i + 1) % 5] != EATING) ) {
                    state[i] = EATING ;
                    self[i].signal () ;
            }
        }
void putdown (int i) {
            state[i] = THINKING;
            // test left and right neighbors
            test((i + 4) % 5);
            test((i + 1) % 5);
      }

      initialization_code() {
            for (int i = 0; i < 5; i++)
            state[i] = THINKING;
        }
}
```

- Each philosopher *I* invokes the operations pickup() and putdown() in the following sequence:

dp.pickup (i)

EAT

dp.putdown (i)

8. State critical section problem? Discuss three solutions to solve the critical section problem.

Answer:

C-S Problem:-

- *n* processes all competing to use some shared data
- each process has a code segment, called critical section, in which the shared data is accessed
- problem – ensure that when one process is executing in its critical section, no other process is allowed to execute in its critical section

Solution to the C-S problem

1. *Mutual Exclusion* – No two processes eat simultaneously

2. *Progress* - If no process eats forever, and some process is hungry, then some (potententially different) hungry process eventually eats.

3. *Bounded Waiting* - A bound exists on the number of times that other processes are allowed to eat after a process P becomes hungry and before process P eats.

- Assume that each process executes at a nonzero speed
- No assumption concerning relative speed of the N processes

9. Describe an algorithm which satisfies all the conditions of critical section problem and also prove how it satisfies all the conditions.

Answer:

```
while (true) {
 flag[i] = TRUE;
 turn = j;
 while ( flag[j] && turn == j);

      CRITICAL SECTION

 flag[i] = FALSE;

       REMAINDER SECTION

}
```

- The two processes share two variables:
  - int turn;
  - Boolean flag[2]
- The variable turn indicates whose turn it is to enter the critical section.
- The flag array is used to indicate if a process is ready to enter the critical section. Flag[i] = true implies that process Pi is ready!
- **Claim: Mutual exclusion is preserved**
  - *Proof:*

1. Assume Pi and Pj in CS at the same time
2. flag[i] & flag[j] == True
   (I) flag[j] & turn == j → False → turn = i

(II) flag[i] & turn == i → False → turn = j

3. turn cannot be i and j at the same time

- **Claim: Progress is met.**
  - *Proof:*
  - Pi stuck at "flag[j] == true & turn == j" while loop
  - (case 1) Pj is not ready to enter
    - flag[j] == false → Pi can enter
  - (case 2) Pj is ready to enter
    - Pj : set flag[j] to true and at its while
    - Observation: turn == i XOR turn == j
    - (case 2.1) turn == i → Pi will enter
    - (case 2.2) turn == j → Pj will enter
      - (case 2.2.1) Pj leaves CS; sets flag[j] to false → Pi enters
      - (case 2.2.2) Pj leaves CS; sets flag[j] to true ;
        - » then sets turn to i → Pi enters
        - » (Pi at while cannot change turn)

- Pi (Pj) will enter the CS (progress) after at most one entry by Pj (Pi) (***bounded waiting***)

10. What is critical section problem and explain two process solutions and multiple process solutions?

Answer:

Critical section problem definition

Two process solutions

Algorithm 1, 2 & 3

Multiple-process solution with algorithm

11. Explain what semaphores are, their usage, implementation given to avoid busy waiting and binary semaphores.

Answer:

Semaphore definition

Usage for mutual exclusion and process synchronization

Implementation to avoid spinlock using block and wakeup

Binary semaphores

12. Write about critical regions and monitors.

Answer:

Critical region definition

Implementation of the conditional-region construct

Monitor definition

Syntax of monitor

Schematic view of monitors

Monitor with condition variables

Monitor solution to dining-philosopher problem

UNIT 3 – DEADLOCK AND MEMORY MANAGEMENT

2 MARKS

1. Define deadlock.

Answer: A process requests resources; if the resources are not available at that time, the process enters a wait state. Waiting processes may never again change state, because the resources they have requested are held by other waiting processes. This situation is called a deadlock.

2. What is the sequence in which resources may be utilized?

Answer: Under normal mode of operation, a process may utilize a resource in the following sequence:

• Request: If the request cannot be granted immediately, then the requesting process must wait until it can acquire the resource.

• Use: The process can operate on the resource.

• Release: The process releases the resource.

3. What are conditions under which a deadlock situation may arise?

Answer: A deadlock situation can arise if the following four conditions hold simultaneously in a system:

a. Mutual exclusion

b. Hold and wait

c. No pre-emption

4. What is a resource-allocation graph?

Answer: Deadlocks can be described more precisely in terms of a directed graph called a system resource allocation graph. This graph consists of a set of vertices V and a set of edges E. The set of vertices V is partitioned into two different types of nodes; P the set consisting of all active processes in the system and R the set consisting of all resource types in the system.

5. Define request edge and assignment edge.

Answer: A directed edge from process Pi to resource type Rj is denoted by Pi->j; it signifies that process Pi requested an instance of resource type Rj and is currently waiting for that resource. A directed edge from resource type Rj to process Pi is denoted by Rj->Pi, it signifies that an instance of resource type has been allocated to a process Pi. A directed edge Pi->Rj is called a request edge. A directed edge R->Pi is called an assignment edge.

6. What are the methods for handling deadlocks?

Answer: The deadlock problem can be dealt with in one of the three ways:

a. Use a protocol to prevent or avoid deadlocks, ensuring that the system will never enter a deadlock state.

b. Allow the system to enter the deadlock state, detect it and then recover.

c. Ignore the problem all together, and pretend that deadlocks never occur in the system.

7. Define deadlock prevention.

Answer: Deadlock prevention is a set of methods for ensuring that at least one of the four necessary conditions like mutual exclusion, hold and wait, no preemption and circular wait cannot hold. By ensuring that that at least one of these conditions cannot hold, the occurrence of a deadlock can be prevented.

8. Define deadlock avoidance.

Answer: An alternative method for avoiding deadlocks is to require additional information about how resources are to be requested. Each request requires the system consider the resources currently available, the resources currently allocated to each process, and the future requests and releases of each process, to decide whether the could be satisfied or must wait to avoid a possible future deadlock.

9. What are a safe state and an unsafe state?

Answer: A state is safe if the system can allocate resources to each process in some order and still avoid a deadlock. A system is in safe state only if there exists a safe sequence. A sequence of processes <P1,P2,....Pn> is a safe sequence for the current allocation state if, for each Pi, the resource that Pi can still request can be satisfied by the current available resource plus the resource held by all the Pj, with j<i. if no such sequence exists, then the system state is said to be unsafe.

10. What is banker's algorithm?

Answer: Banker's algorithm is a deadlock avoidance algorithm that is applicable to a resource-allocation system with multiple instances of each resource type. The two algorithms used for its implementation are:

a. *Safety algorithm*: The algorithm for finding out whether or not a system is in a safe state.

b. *Resource-request algorithm*: if the resulting resource allocation is safe, the transaction is completed and process Pi is allocated its resources. If the new state is unsafe Pi must wait and the old resource-allocation state is restored.

11. Define logical address and physical address.

Answer: An address generated by the CPU is referred as logical address. An address seen by the memory unit that is the one loaded into the memory address register of the memory is commonly referred to as physical address.

12. What is logical address space and physical address space?

Answer: The set of all logical addresses generated by a program is called a logical address space; the set of all physical addresses corresponding to these logical addresses is a physical address space.

13. What is the main function of the memory-management unit?

Answer: The runtime mapping from virtual to physical addresses is done by a hardware device called a memory management unit (MMU).

14. Define dynamic loading.

Answer: To obtain better memory-space utilization dynamic loading is used. With dynamic loading, a routine is not loaded until it is called. All routines are kept on disk in a relocatable load format. The main program is loaded into memory and executed. If the routine needs another routine, the calling routine checks whether the routine has been loaded. If not, the relocatable linking loader is called to load the desired program into memory.

15. Define dynamic linking.

Answer: Dynamic linking is similar to dynamic loading, rather that loading being postponed until execution time, linking is postponed. This feature is usually used with system libraries, such as language subroutine libraries. A stub is included in the image for each library-routine reference. The stub is a small piece of code that indicates how to locate the appropriate memory-resident library routine, or how to load the library if the routine is not already present.

16. What are overlays?

Answer: To enable a process to be larger than the amount of memory allocated to it, overlays are used. The idea of overlays is to keep in memory only those instructions and data that are needed at a given time.

When other instructions are needed, they are loaded into space occupied previously by instructions that are no longer needed.

17. Define swapping.

Answer: A process needs to be in memory to be executed. However a process can be swapped temporarily out of memory to a backing store and

then brought back into memory for continued execution. This process is called swapping.

18. What are the common strategies to select a free hole from a set of available holes?

Answer: The most common strategies are

a. First fit

b. Best fit

c. Worst fit

19. What do you mean by best fit?

Answer: Best fit allocates the smallest hole that is big enough. The entire list has to be searched, unless it is sorted by size. This strategy produces the smallest leftover hole.

20. What do you mean by first fit?

Answer:

First fit allocates the first hole that is big enough .Searching can either start at the beginning of the set of holes or where the previous first-fit search ended. Searching can be stopped as soon as a free hole that is big enough is found.

21. List three examples of deadlocks that are not related to a computer-system environment.

Answer:

_ Two cars crossing a single-lane bridge from opposite directions.

_ A person going down a ladder while another person is climbing up the ladder.

_ Two trains traveling toward each other on the same track.

16 MARKS

1. Consider the following resource-allocation policy. Requests and releases for resources are allowed at any time. If a request for resources cannot be satisfied because the resources are not available, then we check any processes that are blocked, waiting for resources. If they have the desired resources, then these resources are taken away from them and are given to the requesting process. The vector of resources for which the waiting process is waiting is increased to include the resources that were taken away.

For example, consider a system with three resource types and the vector *Available* initialized to (4,2,2). If process *P*0 asks for (2,2,1), it gets them. If *P*1 asks for (1,0,1), it gets them. Then, if *P*0 asks for (0,0,1), it is blocked (resource not available). If *P*2 now asks for (2,0,0), it gets the available one (1,0,0) and one that was allocated to *P*0 (since *P*0 is blocked).

***P*0's *Allocation* vector goes down to (1,2,1), and its *Need* vector goes up to (1,0,1).**

a. Can deadlock occur? If so, give an example. If not, which necessary condition cannot occur?

b. Can indefinite blocking occur?

Answer:

a. Deadlock cannot occur because preemption exists.

b. Yes. A process may never acquire all the resources it needs if they are continuously preempted by a series of requests such as those of process *C*.

2. Explain the difference between internal and external fragmentation.

Answer:

Internal Fragmentation is the area in a region or a page that is not used by the job occupying that region or page. This space is unavailable for use by the system until that job is finished and the page or region is released.

3. Describe the following allocation algorithms:

a. First fit

b. Best fit

c. Worst fit

Answer:

a. First-fit: search the list of available memory and allocate the first block that is big enough.

b. Best-fit: search the entire list of available memory and allocate the smallest block that is big enough.

c. Worst-fit: search the entire list of available memory and allocate the largest block.

(The justification for this scheme is that the leftover block produced would be larger and potentially more useful than that produced by the best-fit approach.)

4. Given memory partitions of 100K, 500K, 200K, 300K, and 600K (in order), how would each of the First-fit, Best-fit, and Worst-fit algorithms place processes of 212K, 417K, 112K, and 426K (in order)? Which algorithm makes the most efficient use of memory?

Answer:

a. First-fit:

b. 212K is put in 500K partition

c. 417K is put in 600K partition

d. 112K is put in 288K partition (new partition 288K = 500K - 212K)

e. 426K must wait

f. Best-fit:

g. 212K is put in 300K partition

h. 417K is put in 500K partition

i. 112K is put in 200K partition

j. 426K is put in 600K partition

k. Worst-fit:

l. 212K is put in 600K partition

m. 417K is put in 500K partition

n. 112K is put in 388K partition

o. 426K must wait

In this example, Best-fit turns out to be the best.

5. Consider a paging system with the page table stored in memory.

a. If a memory reference takes 200 nanoseconds, how long does a paged memory reference take?

b. If we add associative registers, and 75 percent of all page-table references are found in the associative registers, what is the effective memory reference time? (Assume that finding a page-table entry in the associative registers takes zero time, if the entry is there.)

Answer:

a. 400 nanoseconds; 200 nanoseconds to access the page table and 200 nanoseconds to access the word in memory.

b. Effective access time = 0.75 _ (200 nanoseconds) + 0.25 _ (400 nanoseconds) = 250 nanoseconds.

6. Why are segmentation and paging sometimes combined into one scheme?

Answer: Segmentation and paging are often combined in order to improve upon each other. Segmented paging is helpful when the page table becomes

very large. A large contiguous section of the page table that is unused can be collapsed into a single segment table entry with a page-table address of zero. Paged segmentation handles the case of having very long segments that require a lot of time for allocation. By paging the segments, we reduce wasted memory due to external fragmentation as well as simplify the allocation.

7. Consider the following segment table:

Segment	Base	Length
0	**219**	**600**
1	**2300**	**14**
2	**90**	**100**
3	**1327**	**580**
4	**1952**	**96**

What are the physical addresses for the following logical addresses?

a. 0,430

b. 1,10

c. 2,500

d. 3,400

e. 4,112

Answer:

a. 219 + 430 = 649

b. 2300 + 10 = 2310

c. illegal reference, trap to operating system

d. 1327 + 400 = 1727

e. illegal reference, trap to operating system

8. Explain about deadlock prevention?

Answer: In order for the occurrence of deadlock, the four conditions such as mutual exclusion, hold and wait, no preemption and circular wait must occur. By ensuring that one of these conditions cannot hold, we can prevent the occurrence of deadlock.

Mutual exclusion

It must hold for non-sharable resources. For example a printer cannot be simultaneously shared by several processes. Sharable resources do not require mutually exclusive access, and thus cannot be involved in deadlock. Read-only files are a good example of a sharable resource.

Hold and wait

To ensure that hold and wait condition never occurs in the system, we must guarantee that, whenever a process requests a resource, it does not hold any other resources. The protocols used are

1. Each process is to be request and be allocated all its resources before it begins execution.

2. Allows a process to request some resources only when the process has none (no other resources).

Example: A process copies data from a tape drive to a disk file, sorts the disk file and then prints the result.

These protocols have two main disadvantages.

1. Resource utilization may be low, since many of the resources may be allocated but unused for a long period.

2. Starvation (need) is possible. A process that needs several popular resources may have to wait indefinitely, because at least one of the resources that it needs is always allocated to some other processes.

No preemption

There is no preemption of resources that have already been allocated. The protocols used are

1. 1. If a process is holding some resources and requests another resource that cannot be immediately allocated to it, then all resources currently being held are preempted. In other words, these resources are implicitly released. The process will be restarted only when it can regain its old resources, as well as the new one that it is requesting.

2. If a process requests some resources, we first check whether they are available. If they are, we allocate them. If they are not available, we check whether they are allocated to some other process that is waiting for additional resources. If so, we preempt the desired resources from the waiting process and allocate them to the requesting process. If both conditions are not satisfied, the requesting process must wait.

Circular wait

One way to ensure that that this condition never holds is to impose a total ordering of all resource types, and to require that each process requests resources in an increasing ordering of enumeration. The protocols used to prevent deadlock are

1. Each process can request resources only in an increasing order of enumeration.

2. Whenever a process requests an instance of resource type Rj, it has released any resources Ri such that F(Ri)>=F(Rj)

If these two protocols are used, then the circular-wait condition cannot hold.

The function F should be defined according to the normal order of usage of the resources in a system.

9. Briefly discuss on Bankers algorithm?

Answer: The resource-allocation graph algorithm is not applicable to a resource-allocation system with multiple instances for each resource type. So we go for bankers algorithm but is less efficient that resource allocation graph scheme.

When a new process enters it must declare the maximum number of instances of each resource type that it may need. When a user request a set of resources, the system must determine whether the allocation of these resource will leave the system in a safe state. If it will the resources are allocated; otherwise the process must wait until some other process releases enough resources.

Let n be the number of processes in the system and m be the number of resource type. The data structure is

- Available: A vector of length m indicates the number of available resources of each type. If Available[j] = k, there are k instances of resource type Rj available.
- Max: An n x m matrix defines maximum demand of each process. If Max[i,j] = k, then process Pi may request at most k instances of resource type Rj.
- Allocation: A matrix defines the number of resources of each type currently allocated to each process. If Allocation[i,j] = k, then process Pi is currently allocated k instances of resource type Rj.
- Need: a matrix indicates the remaining resource need of each process. If Need[i,j] = k, then process Pi may need k more instances of resource type Rj to complete its task.

  Need[i,j] = Max[i,j] – Allocatoin [i,j]

To simplify the presentation of the banker's algorithm, a notation is established. Let X and Y be the vectors of length n. We say that $X \leq Y$ if and only if $X[i] \leq Y[i]$ for all I = 1,2,…,n.

Safety algorithm

This algorithm is for finding out whether or not a system is in a safe state.

1. Let Work and Finish be vectors of length m and n, respectively. Initialize Work := Available and Finish[i] := false for I = 1,2,….,n.
2. Find an i such that both

    a. Finish[i] = false
    b. $Need_i \leq Work$
3. Work := Work + $Allocation_i$
   Finish[i] := true
   Go to step 2.
4. If Finish[i] = true for all I, then the system is in a safe state.

10. Explain about deadlock detection?

Answer: In deadlock situation, the system must provide

- An algorithm that examines the state of the system to determine whether a deadlock has occurred.
- An algorithm to recover from the deadlock.

Single instance of each resource type

If all resources have only a single instance, then we can define a deadlock detection algorithm that uses a variant of the resource-allocation graph, called a wait-for graph.

An edge from Pi to Pj in a wait-for graph implies that process Pi is waiting for process Pj to release a resource that Pi needs. An edge Pi -> Pj exists in a wait-for graph if and only if the corresponding resource-allocation graph contain two edges Pi -> Rq and Rq -> Pj for some resource Rq.

A deadlock exists in the system if and only if the wait-for graph contains a cycle.

Several instance of a resource

The algorithm for this employs several time-varying data structures. They are

._Available: A vector of length m indicates the number of available resources of each type.

._Allocation: A matrix defines the number of resources of each type currently allocated to each process.

._Request: An n x m matrix indicates the current request of each process.

The algorithm is as follows

1. Let Work and Finish be vectors of length m and n, respectively. Initialize Work := Available. For i = 1,2,…,n, if $Allocation_i \neq 0$, then Finis[i] := false. Otherwise , Finish[i] := true.

2. Find an index i such that both

   a. Finish[i] = false
   b. $Request_i \leq Work$

   If no such i exists, go to step 4.

3. Work := Work + $Allocation_i$
   Finish[i] := true
   Go to step 2.

4. If Finish[i] = false for some i, $1 \leq i \leq n$, then the system in a deadlock state. Moreover if Finish[i] = false, then process Pi is deadlocked.

11. Explain about paging?

Answer: Paging is a memory-management scheme that permits the physical-address space of process to be noncontiguous. Paging avoids the considerable problem of fitting the varying-sized memory chunks onto the backing store.

Recent designs have implement paging by closely integrating the hardware and other operating system.

Basic method

Physical memory is broken into fixed-sized blocks called frames. Logical memory is also broken into blocks of the same size called pages. When a process is to be executed, its pages are loaded into any available memory frames.

Every address generated by the CPU is divided into two parts: a page number (p) and a page offset (d). The page number is used as an index into a

page table. The page table contains the base address of each page in physical memory. This base address is combined with the page offset to define the physical memory address that is sent to the memory unit.

The page size is defined by the hardware. The size of page is typically a power of 2, varying between 512 bytes and 16 MB per page. The logical address is as follows

Page number	Page offset
P	D
m-n	n

m-n denotes the high order bits of a logical address. n low order bits.

Example

If pages are 2,048 bytes, a process of 72,766 bytes would need 35 pages plus 1,086 bytes.

Some CPUs and kernels even support multiple page sizes. For instance, Solaris uses 8 KB and 4MB page sizes, depending on the data stored by the pages.

The operating system is aware of the allocation details of physical memory: which frames are allocated, which frames are available, how many total frames there are and so on. This information is generally kept in a data structure called a frame table.

If a user makes a system call and provides to produce the correct physical address. The operating system maintains a copy of the page table for each processes, just as it maintains a copy of instruction counter and register contents. This copy is used to translate logical addresses to physical address. Paging therefore increases the context-switch time.

Hardware support

The hardware implementation of the page table can be done in several ways. The simplest case, the page table is implemented as a set of dedicated registers. These registers should be built with very high-speed logic to make the paging-address translation efficient.

The usage of registers for the page table is satisfactory if the page table is reasonably small. Most computes must allow page table to be very large. For these machines the page table is kept in main memory, and a page table base register (PTBR) points to the page table. The problem with this approach is the time required to access a user memory location.

A solution to this problem is to use a special, small, fast-lookup hardware cache, called ***translation look-aside buffer*** (TLB). The TLB is associative, high-speed memory. Each entry in the TLB consists of two parts: a key and a value. The TLB contains a few of the page-table entries. When a logical address is generated by the CPU, its page number is presented to the TLB. If the page number is found, its frame number is immediately available and is used to access memory.

If the page number is not in the TLB, a memory reference to the page table must be made. When the frame number is obtained, we can use it to access memory.

The percentage of times that a particular page number is found in the TLB is called hit ratio. To find effective memory-access time, we must weight each case by its probability.

Protection

Memory protection is accomplished by protection bits that area associated with each frame. Normally, these bits are kept in the page table. One bit can define a page to be read-or write or read only. One more bit is generally attached to each entry in the page table: a valid-invalid bit. When the bit is

set to “valid”, this value indicates that the associated page is in the process logical-address space, and is thus a legal page. If the bit is set to “invalid”, this value indicates that the page is not the process logical-address space.

Some system provides hardware in the form of a page-table length register (PTLR) to indicate the size of the page table.

12. Briefly discuss on the structure of page table?

Answer: *1. Hierarchical paging*

One way is to use a two-level paging algorithm, in which the page table itself is also paged. A logical address is divided into a page number and a page offset. The page number is further divided into a 10-bit page number and a 10 bit page offset. Thus a logical address is

Page number		Page offset
P2	P2	D
10	10	12

The address translation method for this architecture works from the outer page table inwards, this scheme is also known as forward-mapped page table. The Pentium II uses this architecture.

2. Hashed page tables

A common approach for handling address spaces larger than 32 bits is to use a hashed page table. Each entry in the hash table contains a linked list of elements that hash to the same location.

Each element consist of three fields

a) The virtual page number

b) The value of the mapped page frame

c) A pointer to the next element in the linked list.

The algorithm works as follows: The virtual page number in the virtual address is hashed into the hash table. The virtual page number is compared to field (a) in the first element in the linked list.

If there is a match, the corresponding page frame is used to form the desired physical address. If there is no match, subsequent entries in the linked list are searched for a matching virtual page number.

A variation to this scheme that is favorable for 64-bit address spaces has been proposed.

Clustered page tables are similar to hashed page tables except that each entry in the hash table refers to several pages rather than single page.

3. Inverted page table

In page table the page table has one entry for each page that the process is using. The operating system must translate this reference into a physical memory address. One of the drawbacks of this method is that each page table may consist of millions of entries.

To solve this problem, we can use an inverted page table. An inverted page table has one entry for each real page of memory. Each entry consists of the virtual address of the page stored in that real memory location; with information about the process that owns that page.

Each virtual address in the system consists of a triple < process-id, page-number, offset>

Each inverted page-table entry is a pair <process-id, page-number> where the process-id assumes the role of the address-space identifier. Although this scheme decreases the amount of memory needed to store each page table, it increases the amount of time needed to search the table when a page reference occurs.

13. Illustrate Bankers algorithm with example

Answer: Banker's Algorithm - Example

Given: 5 processes: p0, p1, p2, p3, p4
3 resource types: A, B, C
A has 10 instances
B has 5 instances
C has 7 instances

Total Resource Vector = TRV = [10, 5, 7]

Resource-Allocation State:

Process	Allocation ABC	MAX ABC	Available ABC	Need = MAX - Allocation ABC
p0	0 1 0	7 5 3	3 3 2	7 4 3
p1	2 0 0	3 2 2	= [10, 5, 7] - [7, 2, 5]	1 2 2
p2	3 0 2	9 0 2		6 0 0
p3	2 1 1	2 2 2		0 1 1
p4	0 0 2	4 3 3		4 3 1

Total Alloc:	7 2 5			

Show that this is a Safe State using the safety algorithm:
Initialization:
work = available = [3 3 2]
finish = 0 0 0 0 0
Notation: ">" means "NOT <="

Search for a safe sequence:
p0: need0 = 7 4 3 > work = 3 3 2, doesn't work - try later, finish = 0 0 0 0 0
p1: need1 = 1 2 2 <= work = 3 3 2, finish = 0 1 0 0 0, work = 3 3 2 + 2 0 0 = 5 3 2
p2: need2 = 6 0 0 > work = 5 3 2, doesn't work - try later, finish = 0 1 0 0 0
p3: need3 = 0 1 1 <= work = 5 3 2, finish = 0 1 0 1 0, work = 5 3 2 + 2 1 1 = 7 4 3
p4: need4 = 4 3 1 <= work = 7 4 3, finish = 0 1 0 1 1, work = 7 4 3 + 0 0 2 = 7 4 5
p2: need2 = 6 0 0 <= work = 7 4 5, finish = 0 1 1 1 1, work = 7 4 5 + 3 0 2 = 10, 4, 7
p0: need0 = 7 4 3 <= work = 10,4,7 finish = 1 1 1 1 1, work = 10 4 7 + 0 1 0 = 10, 5, 7

State is Safe:
Sequence is <p1, p3, p4, p2, p0>
Solution is not unique:
Alternate Safe Sequence: <p1, p3, p4, p0, p2> ... reverse p0 and p2

14. Explain the basic concepts of segmentation.

Answer: User view of program

Segmentation definition

Hardware used with diagram-segment table, base, limit & offset

Protection and sharing with diagram

Fragmentation

UNIT 4 – VIRTUAL MEMORY, FILE SYSTEM INTERFACE

2 MARKS

1. What is virtual memory?

Answer: Virtual memory is a technique that allows the execution of processes that may not be completely in memory. It is the separation of user logical memory from physical memory. This separation provides an extremely large virtual memory, when only a smaller physical memory is available.

2. What is Demand paging?

Answer: Virtual memory is commonly implemented by demand paging. In demand paging, the pager brings only those necessary pages into memory instead of swapping in a whole process. Thus it avoids reading into memory pages that will not be used anyway, decreasing the swap time and the amount of physical memory needed.

3. Define lazy swapper.

Answer: Rather than swapping the entire process into main memory, a lazy swapper is used. A lazy swapper never swaps a page into memory unless that page will be needed.

4. What is a pure demand paging?

Answer: When starting execution of a process with no pages in memory, the operating system sets the instruction pointer to the first instruction of the process, which is on a non-memory resident page, the process immediately faults for the page. After this page is brought into memory, the process continues to execute, faulting as necessary until every page that it needs is in memory. At that point, it can execute with no more faults. This schema is pure demand paging.

5. Define effective access time.

Answer: Let p be the probability of a page fault (0£p£1). The value of p is expected to be close to 0; that is, there will be only a few page faults. The effective access time is Effective access time = (1-p) * ma + p * page fault time. ma : memory-access time

6. Define secondary memory.

Answer: This memory holds those pages that are not present in main memory. The secondary memory is usually a high speed disk. It is known as the swap device, and the section of the disk used for this purpose is known as swap space.

7. What is the basic approach of page replacement?

Answer: If no frame is free is available, find one that is not currently being used and free it. A frame can be freed by writing its contents to swap space, and changing the page table to indicate that the page is no longer in memory. Now the freed frame can be used to hold the page for which the process faulted.

8. What are the various page replacement algorithms used for page replacement?

Answer:

• FIFO page replacement

• Optimal page replacement

• LRU page replacement

• LRU approximation page replacement

• Counting based page replacement

• Page buffering algorithm.

9. What are the major problems to implement demand paging?

Answer: The two major problems to implement demand paging is developing

a. Frame allocation algorithm

b. Page replacement algorithm

10. What is a reference string?

Answer: An algorithm is evaluated by running it on a particular string of memory references and computing the number of page faults. The string of memory reference is called a reference string.

11. What is a file?

Answer: A file is a named collection of related information that is recorded on secondary storage. A file contains either programs or data. A file has certain "structure" based on its type.

12. List the various file attributes.

Answer: A file has certain other attributes, which vary from one operating system to another, but typically consist of these: Name, identifier, type, location, size, protection, time, and date and user identification

13. What are the various file operations?

Answer:

The six basic file operations are

• Creating a file

• Writing a file

• Reading a file

• Repositioning within a file

• Deleting a file

• Truncating a file

14. What is the information associated with an open file?

Answer: Several pieces of information are associated with an open file which may be:

• File pointer

• File open count

• Disk location of the file

• Access rights

15. What are the different accessing methods of a file?

Answer: The different types of accessing a file are:

• *Sequential access*: Information in the file is accessed sequentially

• *Direct access*: Information in the file can be accessed without any particular order.

• *Other access methods*: Creating index for the file, indexed sequential access method (ISAM) etc.

16. What is Directory?

Answer: The device directory or simply known as directory records information-such as name, location, size, and type for all files on that particular partition. The directory can be viewed as a symbol table that translates file names into their directory entries.

17. What are the operations that can be performed on a directory?

Answer: The operations that can be performed on a directory are

• Search for a file

• Create a file

• Delete a file

• Rename a file

• List directory

• Traverse the file system

18. What are the most common schemes for defining the logical structure of a directory?

Answer: The most common schemes for defining the logical structure of a directory

• Single-Level Directory

• Two-level Directory

• Tree-Structured Directories

• Acyclic-Graph Directories

• General Graph Directory

19. Define UFD and MFD.

Answer: In the two-level directory structure, each user has her own user file directory (UFD). Each UFD has a similar structure, but lists only the files of a single user. When a job starts the system's master file directory (MFD) is searched. The MFD is indexed by the user name or account number, and each entry points to the UFD for that user.

20. What is a path name?

Answer:

A pathname is the path from the root through all subdirectories to a specified file. In a two-level directory structure a user name and a file name define a path name.

21. Under what circumstances do page faults occur? Describe the actions taken by the operating system when a page fault occurs.

Answer: A page fault occurs when an access to a page that has not been brought into main memory takes place. The operating system verifies the memory access, aborting the program if it is invalid. If it is valid, a free frame is located and I/O is requested to read the needed page into the free

frame. Upon completion of I/O, the process table and page table are updated and the instruction is restarted.

22. Consider the following page-replacement algorithms. Rank these algorithms on a five point scale from "bad" to "perfect" according to their page-fault rate. Separate those algorithms that suffer from Belady's anomaly from those that do not.

a. LRU replacement

b. FIFO replacement

c. Optimal replacement

d. Second-chance replacement

Answer:

Rank Algorithm Suffer from Belady's anomaly

1 Optimal - no

2 LRU - no

3 Second-chance - yes

4 FIFO - yes

23. What is a file?

Answer: A named collection of related data defined by the creator, recorded on secondary storage.

24. List sample file types, based on use, on the VAX under VMS.

Answer:

_ source programs (.BAS, .FOR, .COB, .PLI, .PAS, .MAR)

_ data files (.DAT)

_ text files (.TXT)

_ command procedures (.COM)

_ mail files (.MAI)

_ compiler-listing files (.LIS, .LST)

_ object files (.OBJ)

_ executable image files (.EXE)

_ journal files (.JOU)

25. What is a sequential file?

Answer: A file that is read one record or block or parameter at a time in order, based on a tape model of a file.

26. What is direct access?

Answer: A file in which any record or block can be read next. Usually the blocks are fixed length.

27. How does user specify block to be fetched in direct access?

Answer: By specifying the relative block number, relative to first block in file, which is block 0.

28. Can a direct access file be read sequentially? Explain.

Answer: Yes. Keep a counter, *cp*, initially set to 0. After reading record *cp*, increment *cp*.

29. How can an index file be used to speed up the access in direct-access files?

Answer: Have an index in memory; the index gives the key and the disk location of its corresponding record. Scan the index to find the record you want, and then access it directly.

30. Explain what ISAM is.

Answer: Indexed sequential access method. The file is stored in sorted order. ISAM has a master index file, indicating in what part of another index file the key you want is; the secondary index points to the file records. In both cases, a binary search is used to locate a record.

31. List two types of system directories

Answer:

a. Device directory, describing physical properties of files.

b. File directory, giving logical properties of the files.

32. List operations to be performed on directories.

Answer: Search for a file, create a file, delete a file, list a directory, rename a file, traverse the file system.

33. List disadvantages of using a single directory.

Answer: Users have no privacy. Users must be careful in choosing file names, to avoid names used by others. Users may destroy each others' work.

34. What is the MFD? UFD? How are they related?

Answer: MFD is master-file directory, which points to the UFDs. UFD is user-file directory, which points to each of user's files.

35. What advantages are there to this two-level directory?

Answer: Users are isolated from each other. Users have more freedom in choosing file names.

36. What disadvantages are there to this two-level directory?

Answer: Without other provisions, two users who want to cooperate with each other are hampered in reaching each other's files, and system files are inaccessible.

37. How do we overcome the disadvantages of the two-level directory?

Answer: Provide links from one user directory to another, creating path names; system files become available by letting the command interpreter search your directory first, and then the system directory if file needed is not in first directory.

38. What is a file path name?

Answer: A list of the directories, subdirectories, and files we must traverse to reach a file from the root directory.

39. What is an acyclic graph?

Answer: A tree that has been corrupted by links to other branches, but does not have any cyclic paths in it.

40. List ways to share files between directories in operating systems.

Answer:

a. Copy file from one account into another.

b. Link directory entry of "copied" file to directory entry of original file.

c. Copy directory entry of file into account file is "copied" into.

41. What is a general graph?

Answer: A tree structure where links can go from one branch to a node earlier in the same branch or other branch, allowing cycles.

42. What problems arise if the directory structure is a general graph?

Answer: Searching for a particular file may result in searching the same directory many times. Deletion of the file may result in the reference count to be nonzero even when no directories point to that file.

16 MARKS

1. Consider the following page reference string:

1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6.

How many page faults would occur for the following replacement algorithms, assuming one, two, three, four, five, six, or seven frames? Remember all frames are initially empty, so your first unique pages will all cost one fault each.

_ LRU replacement

_ FIFO replacement

_ Optimal replacement

Answer:

Number of frames	LRU	FIFO	Optimal

1	20	20	20
2	18	18	15
3	15	16	11
4	10	14	8
5	8	10	7
6	7	10	7
7	7	7	7

2. A page-replacement algorithm should minimize the number of page faults. We can do this minimization by distributing heavily used pages evenly over all of memory, rather than having them compete for a small number of page frames. We can associate with each page frame a counter of the number of pages that are associated with that frame. Then, to replace a page, we search for the page frame with the smallest counter.

a. Define a page-replacement algorithm using this basic idea. Specifically address the problems of

(1) What the initial value of the counters is,

(2) When counters are increased,

(3) When counters are decreased, and

(4) How the page to be replaced is selected.

b. How many page faults occur for your algorithm for the following reference string, for four page frames?

1, 2, 3, 4, 5, 3, 4, 1, 6, 7, 8, 7, 8, 9, 7, 8, 9, 5, 4, 5, 4, 2.

c. What is the minimum number of page faults for an optimal page-replacement strategy for the reference string in part b with four page frames?

Answer:

a. Define a page-replacement algorithm addressing the problems of:

i. Initial value of the counters—0.

ii. Counters are increased—whenever a new page is associated with that frame.

iii. Counters are decreased—whenever one of the pages associated with that frame is no longer required.

iv. How the page to be replaced is selected—finds a frame with the smallest counter.

Use FIFO for breaking ties.

b. 14 page faults

c. 11 page faults

3. What is the cause of thrashing? How does the system detect thrashing?

Once it detects thrashing, what can the system do to eliminate this problem?

Answer: Thrashing is caused by under allocation of the minimum number of pages required by a process, forcing it to continuously page fault. The system can detect thrashing by evaluating the level of CPU utilization as compared to the level of multiprogramming.

It can be eliminated by reducing the level of multiprogramming.

4. Consider a system that supports 5000 users. Suppose that you want to allow 4990 of these users to be able to access one file.

a. How would you specify this protection scheme in UNIX?

b. Could you suggest another protection scheme that can be used more effectively for this purpose than the scheme provided by UNIX?

Answer:

a. There are two methods for achieving this:

i. Create an access control list with the names of all 4990 users.

ii. Put these 4990 users in one group and set the group access accordingly. This scheme cannot always be implemented since user groups are restricted by the system.

b. The universe access information applies to all users unless their name appears in the access-control list with different access permission. With this scheme you simply put the names of the remaining ten users in the access control list but with no access privileges allowed.

5. Explain about directory structure?

Answer:

Some systems store millions of files on terabytes of disk. To manage all these data, we need to organize them. This organization is usually done in two parts. First, disks are split into one or more partitions, also known as minidisks in the IBM world or volumes in the PC and Macintosh. Partitions can be thought of as virtual disks. Partitions can also store multiple operating systems, allowing a system to boot and run more than one.

Second, each partition contains information about files within it. This information is kept in entries in a **device directory** or **volume table of contents**. The device directory records information such as name, location, size, and type- for all files on that partition.

The directory can be viewed as a symbol table that translates file names into their directory entries.

Operations that are to be performed on a directory are

o Search for a file: We are able to find all files whose names match a particular pattern.

o Create a file: New files need to be created and added to the directory.

o Delete a file: We want to remove it from the directory.

o List a directory: List the files along with the content of the directory entry.

o Rename a file: The name of the file is changed.

o Traverse the file system: We may wish to access every directory, and every file within a directory structure.

Single-level Directory

All files are constrained in the same directory, which is easy to support and understood. One limitation is when the number of files increases or when the system has more than one user. We must use a unique name.

Two-level directory

In the two-level directory structure each user has own **user file directory** (UFD). When a user jobs starts or a user logs in, the system's **master file directory** (MFD) is searched. The MFD is indexed by user name or account number, and each entry points to the UFD for the user.

Although the two-level directory structure solves the name-collision problem, still have disadvantages. This structure isolates one user form another. A two-level directory can be thought of as a tree, or at least an inverted tree, of height 2.

A special case of file name situation occurs in regard to the system files such as loaders, assemblers, compilers, utility routines, libraries and so on. Copying all the system files would waste an enormous of space.

The standard solution is to complicate the search procedure slightly. A special user directory is defined to contain the system files. Whenever a file name is given to be loaded, the operating system first searches the local UFD. IF the file is found it is used. If it is not found, the system automatically searches the special user directory that contains the file system

files. The sequence of directories searched when a file is named is called the **search path**.

Tree-structured directories

We can generalize the directory structure to a tree of arbitrary height. This allows the user to create their own sub directories and to organize their files accordingly. The tree has a root directory. Every file in the system has a unique path name. A path name is the path from the root, through all the subdirectories, to a specified file. Each user has a current directory. The current directory should contain most of the files that are of current interest to the user. To change directories, a system call is provided that takes a directory name as a parameter and uses it to redefine the current directory.

Path name can be of two types: absolute path names or relative path names. An **absolute path name** begins at the root and allows a path down to the specified file, giving the directory name on the path. A **relative path name** defines a path from the current directory.

If a directory is empty, its entry in its containing directory can simply be deleted.

Thus to delete a directory, the user must first delete all the files in that directory.

Another approach taken by the UNIX rm command is, when a request is made to delete a directory, that entire directory' s files and subdirectories are also to be deleted. With a tree structure directory system, users can access, in addition to their files, the files of other users.

A path to a file in a tree-structured directory can be longer than that in a two-level directory. To allow users to access programs without having to remember these long paths, the Macintosh operating system maintains a file

called the Desktop file, containing the name and location of all executable programs.

Acyclic-graph directories

An **acyclic graph** allows directories to have shared subdirectories and files. The same file or subdirectory may be in two different directories. A shared file is not the same as two copies of the file. With the shared file, only one actual file exists, so any changes made by one person are immediately visible to other. Shared files and subdirectories can be implemented in several ways. In UNIX shared files are implemented by create a new directory entry called a link. A **link** is effectively a pointer to another file or subdirectory.

Another common approach to implementing shared files is simply to duplicate all information about them in both sharing directories.

Several problems are a file may now have multiple absolute path names. Distinct file names may refer to the same file. To traverse the entire file – this problem becomes significant. Another problem involves deletion. When can the space of shared file is reallocated and reused.

In some situation where link is used, the deletion of a link doses not need to affect the original file. Another approach to deletion is to preserve the file until all references to it are deleted. When a link or directory entry is deleted, we remove its entry on the list. The file is deleted when its file-reference list is empty.

The UNIX operating system uses this approach for non symbolic links (or hard links), keeping a reference count in the file information block.

General graph directory

One serious problem with using an acyclic-graph structure is ensuring that there are no cycles. When we add links to an existing tree-structured

directory, the tree structure is destroyed, resulting in a simple graph structure.

If cycles are allowed to exist in the directory, we likewise want to avoid searching any component twice, for reasons of correctness as well as performance. When cycle exists, the reference count may be nonzero, even when it is no longer possible to refer to a directory or file. This anomaly results from the possibility of self-referencing in directory structure. In this case we generally need to use a garbage collection. Garbage collection involves traversing the entire file system marking everything that can be accessed.

6. Explain the various page replacement strategies.

Answer:

Page replacement-basic scheme with diagram

FIFO page replacement

Optimal page replacement

LRU page replacement

LRU approximation page replacement

Counting-based page replacement

Page buffering algorithm

7. What are files and explain the access methods for files?

Answer:

File definition

Attributes, operations and types

Sequential access with diagram

Direct access

Other access methods-index with diagram

8. Explain about demand paging?

Answer:

A demand paging system is similar to a paging system with swapping. Processes reside on secondary memory. When we want to execute a process, we swap it into memory.

Rather than swapping the entire processes into memory, we use a **laze swapper**. A lazy swapper never swaps a page into memory unless that page will be needed.

Basic concepts

When a process is to be swapped in, the pager guesses which pages will be used before the process is swapped out again. Instead of swapping in a whole process, the pager brings only those necessary pages into memory.

The valid-invalid bit scheme can be used to distinguish between pages that are in memory and those pages that are on the disk. Access to a page marked invalid causes a **page-default trap**. This trap is the result of the operating system's failure to bring the desired page into memory.

The procedure for handling the page fault is as follows

1. We check the internal table to determine whether the reference was valid or invalid.
2. If the reference was invalid, we terminate the process.
3. We find a free frame.
4. We schedule a disk operation to read the desired page into the newly allocated frame.
5. When the disk read is complete, modify the internal table to indicate that the page is now in memory.
6. We restart the instruction.

The hardware to support demand paging is as follows

o *Page table*: This table has the ability to mark an entry invalid though a valid-invalid bit or special value of protection bit.

o *Secondary memory*: This memory holds those pages that are not present in main memory. It is a high-speed disk. It is known as swap device, and the section of disk used for this purpose is known as **swap space**.

The major difficulty occurs when one instruction may modify several different locations.

This problem can be solved in two different ways.

In one solution, the microcode computes and attempts to access both ends of both blocks. If a page fault going to occur, it will happen at this step before anything is modified.

The other solution uses temporary registers to hold the values of overwritten locations. If there is a page fault, all the old values are written back into memory before the trap occurs.

A similar architectural problem occurs in machine that uses special addressing modes, including auto decrement and auto increment. These addressing modes use a register as a pointer and automatically decrement or increment the register as indicated.

One solution is to create a new special status register to record the register number and amount modified for any register that is changed during the execution of an instruction.

Performance of demand paging

Demand paging can have a significant effect on the performance of a computer system. As long as we have no page faults, the effective access time is equal to the memory access time. The memory access time is denoted by **ma**, now ranges from 10 to 200 nanoseconds.

Let p be the probability of page fault. We could expect p to be close to zero; that is there will be only a few page faults. The **effective access time** is then

Effective access time = (1 – p) * ma + p * page fault time.

A page fault causes the following sequence to occur.

1. Trap (shut in) to the operating system.
2. Save the process registers and process state.
3. Determine that the interrupt was a page fault.
4. Check that the page reference was legal and determine the location of the page on the disk.
5. Issue a read from the disk to a free frame
6. While waiting, allocate the CPU to some other user.
7. Interrupt fro the disk.
8. Save the registers and process state for the other user.
9. Determine that the interrupt was from disk.
10. Correct the page table and other tables to show that the desired page is now in memory.
11. Wait for the CPU to be allocated to this process again.
12. Restore the registers, process state, and new page table, then resume the interrupted instruction.

We are faced with three major components of the page-fault service time.

1. Service the page-fault interrupts.
2. Read in the page.
3. Restart the processes.

If we take an average page-fault service time of 25 milliseconds and a memory-access time of 100 nanoseconds, then the effective access time in nanoseconds is

Effective access time = (1-p) x (100) + p (25 milliseconds)
= (1-p) x 100 + p x 25,000,000
= 100 + 24,999,900 x p.

9. Explain the various file types and structures?

Answer:

A common technique for implementing file types is to include the type as part of the file name. The name is split into two parts – a name and an extension, usually separated by a period character. The file with a .com, .exe, or .bat extension can be executed. Assembler expects source files to have an .asm extension.

The UNIX system uses a crude **magic number** stored at the beginning of some files to indicate roughly the type of the file – executable program , batch file (or shell script) , postscript file, and so on.

File structure

Certain files must conform to a required structure that is understood by the operating system. The operating system may require that an executable file have a specific structure so that it can determine where in memory to load the file and what location of the first instruction is.

Some operating system imposes a minimal number of file structures. This approach has been adopted in UNIX, MS-DOS and others. UNIX considers each file to be a sequence of 8-bit bytes; no interpretation of these bits is made by the operating system.

The Macintosh operating system supports minimal number of file structures. It expects files to contain two parts: a **resource fork** and a **data fork**. The resource fork contains information of interest to the user. Example it holds the labels of any buttons displayed by the program. A foreign user may want to modify these buttons. The data fork contains program code or data.

Internal file structure

All disk I/O is performed in units of one block, and all blocks are the same size. It is unlikely that the physical record size will exactly match the length of the desired logical record. Logical record may even vary in length. Packing a number of logical records into physical blocks is a common solution to this problem.

The logical record size, physical block size, and packing technique determine how many logical records are in each physical block. Because disk space is always allocated in blocks, some portion of the last block of each file is generally wasted. The wasted byte allocated to keep everything in units of blocks is **internal fragmentation**. All file system suffer from internal fragmentation; the larger the block size, the greater the internal fragmentation.

10. Discuss on LRU approximation page replacement?

Answer:

This algorithm uses reference bit. The reference bit is set by the hardware, whenever that page is referenced.

1. Additional-reference-bits algorithm

We can keep an 8-bit byte for each page in a table in memory. The operating system shifts the reference bits right 1 bit, discarding the low-order bit. These 8 bits sift register contain the history of page used for last eight time periods. A page with a history value of 11000100 has been used more recently than has one with 01110111. The page with the lowest number is the LRU page, and it can be replaced.

2. Second-Chance algorithm

When a page has been selected, we inspect its reference bit. If the value is 0, we proceed to replace this page. If the reference bit is set to 1, however, we

give that page a second chance and move on to select the next FIFO page. Thus pages that given the second chance will not be replaced until all other pages are replaced. One way to implement the second-chance algorithm is as a circular queue. A pointer indicates which page is replaced next. When a frame is needed, the pointer advances until it finds a replaced next. Once a victim page is found, the page is replaced, and the new page is inserted in the circular queue in that position.

3. Enhanced second-chance algorithm.

When we enhance the second-chance algorithm by considering both the reference bit and the modify bit as an order pair. We have the following four possible classes.

a) (0,0) neither recently used nor modified – best page to replace.

b) (0,1) not recently used but modified – not quite as good.

c) (1,0) recently used but clean – it probably will be used again soon.

d) (1,1) recently used and modified – it probably will be used again soon, and the page will be need to be written out to disk before it can be replaced.

This algorithm is used in the Macintosh virtual-memory-management scheme.

11. Briefly discuss on page replacement?

Answer:

Page replacement approach is stated as follows. If no frame is free, we find one that is not currently being used and free it. We can free a frame by writing its contents to swap space, and changing the page table to indicate that the page is no longer in memory. We now use the freed frame. We modify the page-fault service routine

1. Find the location of the desired page on the disk.

2. Find a free frame:

a. If there is a free frame, use it

b. If there is no free frame, uses a page-replacement algorithm to select a victim frame.

c. Write the victim page to the disk; change the page and frame tables accordingly.

3. Read the desired page into the free frame; change the page and frame tables.

4. Restart the user process.

If no frames are free, two page transfers are required. This situation effectively doubles the page-fault service time and increase the effective access time. We can reduce this overhead by using a modify bit (or dirty bit). The modify bit for a page is set by the hardware whenever any word or byte in the page is written into indicating that the page has been modified.

If the bit is set, we know that the page has been modified since it was read in from the disk.

In this case we must write that page to the disk. If the modify bit is not set, however, the page has not been modified since it was read into memory.

Page replacement is basic to demand paging. It completes the separation between logical memory and physical memory. With this mechanism, an enormous virtual memory can be provided for programmers on a smaller physical memory. With demand paging the size of the logical address space is no longer constrained by physical memory.

We must solve two major problems to implement demand paging: we must develop a **frame-allocation algorithm and a page-replacement algorithm.** We evaluate an algorithm by running it on a particular string of memory reference and computing the number of page faults. The string of memory references is called a **reference string**.

FIFO page replacement

A FIFO replacement algorithm associates with each page the time when that page was brought into memory. When a page must be replaced, the oldest page is chosen. We can create a FIFO queue to hold all pages in memory. We replace the page at the head of the queue. Insert page at the last of the queue.

The FIFO page-replacement algorithm is easy to understand and program. However its performance is not always good. Even if we select for replacement a page that is in active use, everything still works correctly. After we page out an active page to bring in a new one, a fault occurs almost immediately to retrieve the active page. Some other pages will be needed to be replaced to bring the active page back into memory. Thus, a bad replacement choice increases the page-fault rate and slows process execution.

When plotting on a graph the page faults versus the number of available frames. We notice that the number of faults for four frames is greater than the number of faults for three frames. This most unexpected result is known as **Belady's anomaly**. That is for some page replacement algorithm, the page fault rate may increase as the number of allocated frames increases.

UNIT 5 – FILE SYSTEM IMPLEMENTATION, DISK SCHEDULING

2 MARKS

1. What are the various layers of a file system?

Answer:

The file system is composed of many different levels. Each level in the design uses the feature of the lower levels to create new features for use by higher levels.

• Application programs

• Logical file system

• File-organization module

• Basic file system

• I/O control

• Devices

2. What are the structures used in file-system implementation?

Answer:

Several on-disk and in-memory structures are used to implement a file system

a. On-disk structure include

· Boot control block

· Partition block

· Directory structure used to organize the files

· File control block (FCB)

b. In-memory structure include

· In-memory partition table

· In-memory directory structure

· System-wide open file table

· Per-process open table

3. What are the functions of virtual file system (VFS)?

Answer:

a. It separates file-system-generic operations from their implementation defining a clean VFS interface. It allows transparent access to different types of file systems mounted locally.

b. VFS is based on a file representation structure, called a vnode. It contains a numerical value for a network-wide unique file .The kernel maintains one vnode structure for each active file or directory.

4. Define seek time and latency time.

Answer:

The time taken by the head to move to the appropriate cylinder or track is called seek time. Once the head is at right track, it must wait until the desired block rotates under the read-write head. This delay is latency time.

5. What are the allocation methods of a disk space?

Answer:

Methods of allocating disk space which are widely in use are

a. Contiguous allocation

b. Linked allocation

c. Indexed allocation

6. What are the advantages of Contiguous allocation?

Answer:

The advantages are

a. Supports direct access

b. Supports sequential access

c. Number of disk seeks is minimal.

7. What are the drawbacks of contiguous allocation of disk space?

Answer:

The disadvantages are

a. Suffers from external fragmentation

b. Suffers from internal fragmentation

c. Difficulty in finding space for a new file

d. File cannot be extended

e. Size of the file is to be declared in advance

8. What are the advantages of Linked allocation?

Answer:

The advantages are

a. No external fragmentation

b. Size of the file does not need to be declared

9. What are the disadvantages of linked allocation?

Answer:

The disadvantages are

a. Used only for sequential access of files.

b. Direct access is not supported

c. Memory space required for the pointers.

d. Reliability is compromised if the pointers are lost or damaged

10. What are the advantages of Indexed allocation?

Answer:

The advantages are

a. No external-fragmentation problem

b. Solves the size-declaration problems.

c. Supports direct access

11. How can the index blocks be implemented in the indexed allocation scheme?

Answer:

The index block can be implemented as follows

a. Linked scheme

b. Multilevel scheme

c. Combined scheme

12. Define rotational latency and disk bandwidth.

Answer:

Rotational latency is the additional time waiting for the disk to rotate the desired sector to the disk head. The disk bandwidth is the total number of bytes transferred, divided by the time between the first request for service and the completion of the last transfer.

13. How free-space is managed using bit vector implementation?

Answer:

The free-space list is implemented as a bit map or bit vector. Each block is represented by 1 bit. If the block is free, the bit is 1; if the block is allocated, the bit is 0.

14. Define buffering.

Answer:

A buffer is a memory area that stores data while they are transferred between two devices or between a device and an application. Buffering is done for three reasons

a. To cope with a speed mismatch between the producer and consumer of a data stream

b. To adapt between devices that have different data transfer sizes

c. To support copy semantics for application I/O

15. Define caching.

Answer:

A cache is a region of fast memory that holds copies of data. Access to the cached copy is more efficient than access to the original. Caching and buffering are distinct functions, but sometimes a region of memory can be used for both purposes.

16. Define spooling.

Answer:

A spool is a buffer that holds output for a device, such as printer, that cannot accept interleaved data streams. When an application finishes printing, the spooling system queues the corresponding spool file for output to the printer. The spooling system copies the queued spool files to the printer one at a time.

17. What are the various disk-scheduling algorithms?

Answer:

The various disk-scheduling algorithms are

a. First Come First Served Scheduling

b. Shortest Seek Time First Scheduling

c. SCAN Scheduling

d. C-SCAN Scheduling

f. LOOK scheduling

18. What is low-level formatting?

Answer:

Before a disk can store data, it must be divided into sectors that the disk controller can read and write. This process is called low-level formatting or physical formatting. Low-level formatting fills the disk with a special data

structure for each sector. The data structure for a sector consists of a header, a data area, and a trailer.

19. What is the use of boot block?

Answer:

For a computer to start running when powered up or rebooted it needs to have an initial program to run. This bootstrap program tends to be simple. It finds the operating system on the disk loads that kernel into memory and jumps to an initial address to begin the operating system execution. The full bootstrap program is stored in a partition called the boot blocks, at fixed location on the disk. A disk that has boot partition is called boot disk or system disk.

20. What is sector sparing?

Answer:

Low-level formatting also sets aside spare sectors not visible to the operating system. The controller can be told to replace each bad sector logically with one of the spare sectors. This scheme is known as sector sparing or forwarding.

21. List three ways of allocating storage, and give advantages of each.

Answer:

a. Contiguous allocation. Fastest, if no changes are to be made. Also easiest for random access files.

b. Linked allocation. No external fragmentation. File can grow without complications.

c. Indexed allocation. Supports direct access without external fragmentation.

22. What is contiguous allocation?

Answer: Allocation of a group of consecutive sectors for a single file.

23. What is preallocation? Why do it?

Answer: Allocating space for a file before creating the file to allow for expansion. This reserves space for a particular file so that other files can't grab it. The new file may initially use only a small portion of this space.

24. What is linked allocation, as detailed in text?

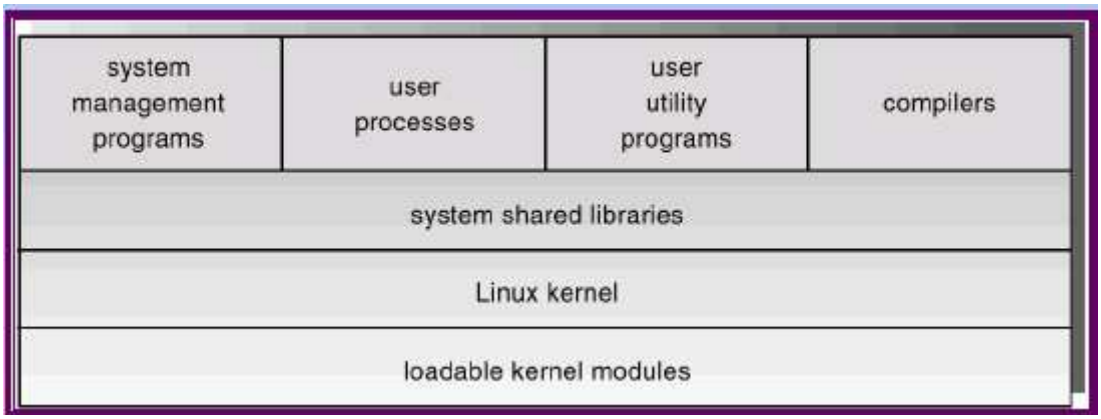
Answer: Directory contains pointers to first and last blocks of file. Each block of file (except last) has pointer to the next block.

25. What is indexed allocation?

Answer: Each file has its own block of pointers to the sectors of the file.

26. Components of LINUX system?

Answer:



16 MARKS

1. Consider a file currently consisting of 100 blocks. Assume that the file control block (and the index block, in the case of indexed allocation) is already in memory. Calculate how many disk I/O operations are required for contiguous, linked, and indexed (single-level) allocation strategies, if, for one block, the following conditions hold. In the contiguous allocation case, assume that there is no room to grow in the

beginning, but there is room to grow in the end. Assume that the block information to be added is stored in memory.

a. The block is added at the beginning.

b. The block is added in the middle.

c. The block is added at the end.

d. The block is removed from the beginning.

e. The block is removed from the middle.

f. The block is removed from the end.

Answer:

	Contiguous	Linked	Indexed
a.	201	1	1
b.	101	52	1
c.	1	3	1
d.	198	1	0
e.	98	52	0
f.	0	100	0

2. Suppose that a disk drive has 5000 cylinders, numbered 0 to 4999. The drive is currently serving a request at cylinder 143, and the previous request was at cylinder 125. The queue of pending requests, in FIFO order, is 86, 1470, 913, 1774, 948, 1509, 1022, 1750, 130 Starting from the current head position, what is the total distance (in cylinders) that the disk arm moves to satisfy all the pending requests, for each of the following disk scheduling algorithms?

a. FCFS

b. SSTF

c. SCAN

d. LOOK

e. C-SCAN

Answer:

a. The FCFS schedule is 143, 86, 1470, 913, 1774, 948, 1509, 1022, 1750, 130. The total seek distance is 7081.

b. The SSTF schedule is 143, 130, 86, 913, 948, 1022, 1470, 1509, 1750, 1774. The total seek distance is 1745.

c. The SCAN schedule is 143, 913, 948, 1022, 1470, 1509, 1750, 1774, 4999, 130, 86. The total seek distance is 9769.

d. The LOOK schedule is 143, 913, 948, 1022, 1470, 1509, 1750, 1774, 130, 86. The total seek distance is 3319.

e. The C-SCAN schedule is 143, 913, 948, 1022, 1470, 1509, 1750, 1774, 4999, 86, 130. The total seek distance is 9813.

f. (Bonus.) The C-LOOK schedule is 143, 913, 948, 1022, 1470, 1509, 1750, 1774, 86, 130. The total seek distance is 3363.

3. Compare the performance of C-SCAN and SCAN scheduling, assuming a uniform distribution of requests. Consider the average response time (the time between the arrival of a request and the completion of that request's service), the variation in response time, and the effective bandwidth. How does performance depend on the relative sizes of seek time and rotational latency?

Answer:

There is no simple analytical argument to answer the first part of this question. It would make a good small simulation experiment for the students. The answer can be found in Figure 2 of Worthington et al. [1994]. (Worthington et al. studied the LOOK algorithm, but similar results obtain for SCAN. Figure 2 in Worthington et al. shows that C-LOOK has an average response time just a few percent higher than LOOK but that C-

LOOK has a significantly lower variance in response time for medium and heavy workloads. The intuitive reason for the difference in variance is that LOOK (and SCAN) tends to favor requests near the middle cylinders, whereas the C-versions do not have this imbalance. The intuitive reason for the slower response time of C-LOOK is the "circular" seek from one end of the disk to the farthest request at the other end. This seek satisfies no requests.

It only causes a small performance degradation because the square-root dependency of seek time on distance implies that a long seek isn't terribly expensive by comparison with moderate length seeks.

For the second part of the question, we observe that these algorithms do not schedule to improve rotational latency; therefore, as seek times decrease relative to rotational latency, the performance differences between the algorithms will decrease.

4. Is disk scheduling, other than FCFS scheduling, useful in a single-user environment? Explain your answer.

Answer: In a single-user environment, the I/O queue usually is empty. Requests generally arrive from a single process for one block or for a sequence of consecutive blocks. In these cases, FCFS is an economical method of disk scheduling. But LOOK is nearly as easy to program and will give much better performance when multiple processes are performing concurrent I/O, such as when a Web browser retrieves data in the background while the operating system is paging and another application is active in the foreground.

5. Explain why SSTF scheduling tends to favor middle cylinders over the innermost and outermost cylinders.

Answer: The center of the disk is the location having the smallest average distance to all other tracks. Thus the disk head tends to move away from the edges of the disk. Here is another way to think of it. The current location of the head divides the cylinders into two groups. If the head is not in the center of the disk and a new request arrives, the new request is more likely to be in the group that includes the center of the disk; thus, the head is more likely to move in that direction.

6. Requests are not usually uniformly distributed. For example, a cylinder containing the file system FAT or inodes can be expected to be accessed more frequently than a cylinder that only contains files. Suppose you know that 50 percent of the requests are for a small, fixed number of cylinders.

a. Would any of the scheduling algorithms discussed in this chapter be particularly good for this case? Explain your answer.

b. Propose a disk-scheduling algorithm that gives even better performance by taking advantage of this "hot spot" on the disk.

c. File systems typically find data blocks via an indirection table, such as a FAT in DOS or inodes in UNIX. Describe one or more ways to take advantage of this indirection to improve the disk performance.

Answer:

a. SSTF would take greatest advantage of the situation. FCFS could cause unnecessary head movement if references to the "high-demand" cylinders were interspersed with references to cylinders far away.

b. Here are some ideas. Place the hot data near the middle of the disk. Modify SSTF to prevent starvation. Add the policy that if the disk becomes idle for more than, say, 50 ms, the operating system generates an

anticipatory seek to the hot region, since the next request is more likely to be there.

c. Cache the metadata in primary memory, and locate a file's data and metadata in close physical proximity on the disk. (UNIX accomplishes the latter goal by allocating data and metadata in regions called *cylinder groups*.)

7. Why is rotational latency usually not considered in disk scheduling? How would you modify SSTF, SCAN, and C-SCAN to include latency optimization?

Answer: Most disks do not export their rotational position information to the host. Even if they did, the time for this information to reach the scheduler would be subject to imprecision and the time consumed by the scheduler is variable, so the rotational position information would become incorrect. Further, the disk requests are usually given in terms of logical block numbers, and the mapping between logical blocks and physical locations is very complex.

8. Explain about file system structure?

Answer:

File system structure have two characteristics they are

1. They can be rewritten in place.
2. They can access directly any given block of information on the disk.

To provide an efficient and convenient access to the disk, the operating system imposes one or more file systems to allow the data to be stored, located and retrieved easily.

A file system poses two quite different design problems. The first problem is defining how the file system should look to the user. The second problem is

creating algorithms and data structures to map the logical file system onto the physical secondary-storage devices.

The file system is composed of many different levels. The structure is

Application programs

Logical file system

File-organization module

Basic file system

I/O control

Devices

The lowest level, the I/O control consists of **device drivers** and interrupts handlers to transfer information between the main memory and the disk systems. A device driver can be thought of as a translator. Its input consists of high-level commands such as “retrieve block 123”.

The **basic file system** needs only to issue generic commands to the appropriate device driver to read and write physical blocks on the disk.

The **file-organization module** knows about files and their logical blocks, as well as physical blocks. It also includes a free-space manager, which tracks unallocated blocks and provides these blocks to the file-organization module when requested.

The **logical file system** manages metadata information. Metadata includes all of the file-system structure, excluding actual data. It maintains file structure via file control blocks.

A **file control block** (FCB) contains information about the file, including ownership, permission, and location of the file contents. The logical file system is also responsible for protection and security.

Most operating systems support more than one file system. Windows NT supports disk file-system formats of FAT, FAT32 and NTFS as well as CD-ROM, DVD and floppy disk file system formats.

9. Briefly explain about file system implementation?

Answer:

Several on-disk and in-memory structures are used to implement a file system. On disk, the file system may contain information about how to boot an operating system stored there, the total number of blocks, the number and the location of free blocks, the directory structure, and individual files.

The on-disk structures include

o A **boot control block** can contain the information needed by the system to boot an operating from that partition. If the disk does not contain an operating system, this block can be empty. It is typically the first block of a partition. In UFS this is called **boots block**. In NTFS it is the **partition boot sector**.

o A partition control block contains partitions details, such as the number of blocks in the partition, size of the blocks, free-blocks and free-block pointers and free FCB count and FCB pointers. In UFS this is called a **super block**. In NTFS it is the Master File Table.

o A directory structure is used to organize the files.

o An FCB contains many of the file' s details, including file permissions, ownership, size, and location of the data blocks. In UFS this is called the inode.

The in-memory information is used for both file-system management and performance improvement via caching. The structure can include

o An in-memory partition table containing information about each mounted partition.

o An in-memory directory structure that holds the directory information of recently accessed directories.

o The **system-wide open-file table** contains a copy of the FCB of each open file, as well as other information.

o The **per-process open-file table** contains a pointer to the appropriate entry in the system wide open-file table as well as other information.

To create a new file, an application program calls the logical file system. The logical file system knows the format of the directory structures. To create a new file, it allocates a new FCB, reads the appropriate directory into memory, and updates it with the new file name and FCB, and writes it back to the disk. A typical file control block is as shown below

File permissions
File dates (create, access, write)
File owner, group, ACL
File size
File data blocks

The open call passes a file name to the file system. Parts of the directory structure are cached in memory to speed directory operations. Next an entry is made in the per-process open-file table, with a pointer in the system-wide open-file table and some other fields. The open call returns a pointer to the appropriate entry in the per-process file system table. All the file operations are performed via this pointer. The name given to the index varies. UNIX system refers to it as a **file descriptor**. Windows 2000 refers to it as a **file handle**.

When a process closes the file, the per-processes table entry is removed, and the system-wide entry's open count is decremented.

Using the caching aspects, all information about the open file, except for its actual data blocks is in memory.

Partitions and mounting

A disk can be sliced into multiple partitions, or a partition can span multiple disks.

Each partition can be either “raw”, containing no file system, or “cooked” containing a file system. **Raw disk** is used where no file system is appropriate. Raw disk can also hold information needed by disk RAID systems, such as bit maps indicating which blocks are mirrored and which have changed and needed to be mirrored.

Boot information can be stored in a separate partition. It has its own format.

Execution of the image stars at a predefined location, such as the first byte. This boot image contain more than the instructions for how to boot a specific operating system. PCs and other systems can be **dual-booted**. Multiple operating systems can be installed on such system.

The **root partition**, which contains the operating-system kernel and potentially other system files, is mounted at boot time. In successful mount operation, operating system verifies that the device contains a valid file system. Finally the operating system notes in its in-memory **mount table** structure that a file system is mounted, and the type of the file system.

On UNIX file systems can be mounted at any directory. This is implemented by setting a flag in the in-memory copy of the inode for that directory.

Virtual file systems

The file-system implementation consists of three major layers. The first layer is the file-system interface, based on the open, read, write and close calls and file descriptors.

The second layer is called the **Virtual File System** (VFS). It serves two important functions.

1. It separates file-system-generic operations from their implementation by defining a clean VFS interface.
2. The VFS is based on a file-representation structure called a vnode, which contains a numerical designator for a network-wide unique file. This network-wide uniqueness is required for support of network file systems.

10. Explain about file allocation methods?

Answer:

The main problem in direct-access nature is how to allocate space to these files so that disk space if utilized effectively and files can be accessed quickly. Three major methods are used; they are contiguous, linked and indexed.

Contiguous allocation

The contiguous-allocation method requires each file to occupy a set of contiguous blocks of the disk. Disk addresses define a linear ordering on the disk. Thus the number of disks seeds required for accessing contiguously allocated files is minimal. The IBM VM/CMS operating system uses contiguous allocation because it provides such good performance.

Contiguous allocation of a file is defined by the disk address and length of the first block. The directory entry for each file indicates the address of the starting block and the length of the area allocated for this file.

Contiguous allocation has some problems. One difficulty is finding space for a new file. The contiguous disk-space-allocation problem can be seen to be a particular application of the general **dynamic storage-allocation** problem. First fit and best fit are the most common strategies used to select a free hole from the set of available holes.

These algorithms suffer from the problem of **external fragmentation**.

Linked allocation

With linked allocation, each file is a linked list of disk blocks; the disk blocks may be scattered anywhere on the disk. The directory contains a pointer to the first and last blocks of the file.

Indexed allocation

Indexed allocation bringing all the pointers together into one location: the index block. Each file has its own index block, which is an array of disk-block addresses. The ith entry in the index block points to eh ith block of the file. The directory contains the address of the index block.

11. Briefly discuss on I/O hardware?

Answer:

A controller is a collection of electronics that can operate a port, a bus, or a device. A serial-port controller is a simple controller. It is a single chip in the computer that controls the signals the signal on the wires of a serial port.

The device control registers are mapped into the address space of the processor. The CPU executes i/o requests using the standard data transfer instructions to read and write the device-control registers.

An I/O port consist of

a. Status register

b. Control register

c. Data-in register

d. Data-out register

Polling – (also refer book)

Interrupts

The hardware mechanism that enables a device to notify the CPU is called an interrupt. The basic interrupt mechanism works as follows. The CPU

hardware has a wire called the interrupt-request line that the CPU senses after executing every instruction. When the CPU detects that a controller has asserted a signal on the interrupt request line, the CPU saves a small amount of state, such as the current value of instruction pointer, and jumps to the interrupt-handler routine at a fixed address in memory.

Direct memory access

Many computers avoid burdening the main CPU with programmed I/O by offloading sine if this work to a special-purpose processor called a direct memory address controller.

12. Explain about disk scheduling with neat diagram? (Also refer book)

Answer:

FCFS Scheduling

SSTF scheduling

SCAN scheduling

C-SCAN scheduling

LOOK Scheduling

13. Discuss Disk management and swap space management?

Answer: REFER BOOK

14. The Linux scheduler implements *soft* real-time scheduling. What features are missing that is necessary for some real-time programming tasks? How might they be added to the kernel?

Answer:

Linux's "soft" real-time scheduling provides ordering guarantees concerning the priorities of runnable processes: real-time processes will always be given a higher priority by the scheduler than normal time-sharing processes, and a real-time process will never be interrupted by another process with a lower real-time priority.

However, the Linux kernel does not support “hard” real-time functionality. That is, when a process is executing a kernel service routine, that routine will always execute to completion unless it yields control back to the scheduler either explicitly or implicitly (by waiting for some asynchronous event). There is no support for preemptive scheduling of kernel mode processes. As a result, any kernel system call that runs for a significant amount of time without rescheduling will block execution of any real-time processes.

Many real-time applications require such hard real-time scheduling. In particular, they often require guaranteed worst-case response times to external events. To achieve these guarantees and to give user-mode real time processes a true higher priority than kernel mode lower-priority processes, it is necessary to find a way to avoid having to wait for low-priority kernel calls to complete before scheduling a real-time process. For example, if a device driver generates an interrupt that wakes up a high-priority real-time process, then the kernel needs to be able to schedule that process as soon as possible, even if some other process is already executing in kernel mode.

Such preemptive rescheduling of kernel-mode routines comes at a cost. If the kernel cannot rely on non-preemption to ensure atomic updates of shared data structures, then reads of or updates to those structures must be protected by some other, finer-granularity locking mechanism. This fine-grained locking of kernel resources is the main requirement for provision of tight scheduling guarantees.

Many other kernel features could be added to support real-time programming. Dead line based scheduling could be achieved by making modifications to the scheduler. Prioritization of IO operations could be implemented in the block-device IO request layer.

15. The Linux kernel does not allow paging out of kernel memory. What effect does this restriction have on the kernel's design? What are two advantages and two disadvantages of this design decision?

Answer:

The primary impact of disallowing paging of kernel memory in Linux is that the non-preemptability of the kernel is preserved. Any process taking a page fault, whether in kernel or in user mode, risks is being rescheduled while the required data is paged in from disk. Because the kernel can rely on not being rescheduled during access to its primary data structures, locking requirements to protect the integrity of those data structures are very greatly simplified. Although design simplicity is a benefit in itself, it also provides an important performance advantage on uni-processor machines due to the fact that it is not necessary to do additional locking on most internal data structures.

There are a number of disadvantages to the lack of pageable kernel memory, however. First of all, it imposes constraints on the amount of memory that the kernel can use. It is unreasonable to keep very large data structures in non-pageable memory, since that represents physical memory that absolutely cannot be used for anything else. This has two impacts: first of all, the kernel must prune back many of its internal data structures manually, instead of being able to rely on a single virtual memory mechanism to keep physical memory usage under control. Second, it makes it infeasible to implement certain features that require large amounts of virtual memory in the kernel, such as the /tmpfilesystem (a fast virtual memory based file-system found on some UNIX systems).

Note that the complexity of managing page faults while running kernel code is not an issue here. The Linux kernel code is already able to deal with page

faults: it needs to be able to deal with system calls whose arguments reference user memory which may be paged out to disk.

MODEL AND UNIVERSITY QUESTION PAPERS

MODEL QUESTION PAPER # 1
V SEMESTER
CS1252 – OPERATING SYSTEMS

Time: Three Hours **Maximum : 100 Marks**

Answer All The Questions

PART – A (10 x 2 = 20 Marks)

1. List the responsibilities of the operating system in connection with disk management.
2. Differentiate between tightly coupled and loosely coupled system.
3. State what does a thread share with peer threads?
4. What is a context switching? Discuss
5. Define internal fragmentation.
6. What data type is a file?
7. List the four conditions for deadlock.
8. Discuss the terms: Logical address; Physical address.
9. In the context of disk scheduling define seek time.
10. In the context of disk reliability define mirroring.

PART – B (5 x 16 = 80 Marks)

11.a) i) Explain how hardware protection can be achieved.(7)
ii) Explain long term, medium and short term scheduler. (6)
iii) What is a real time system? (3)

OR

11.b) i) Discuss in detail about inter process communication. (8)
ii) Explain how parameters can be passed to system calls. (8)

12.a) Discuss the critical section problem, solving the dining philosopher' problem using semaphores.

OR

12.b) Consider the following set of processes, with the length of the CPU-burst time given in milliseconds

Process	Burst Time	Priority
P1	10	3
P2	1	1
P3	2	3
P4	1	4
P5	5	2

The processes are assumed to have arrived in the order P1, P2, P3, P4, and P5 all at time 0.

a. Draw four Gantt charts illustrating the execution of these processes using FCFS, SJF, a nonpreemptive priority (a smaller priority number implies a higher priority), and RR (quantum=1) scheduling.
b. What is the turnaround time of each process for teach of the scheduling algorithms in part a?
c. What is the waiting time of each process for each of the scheduling algorithms in part a?
d. Which of the schedules in part a results in the minimal average waiting time(over all processes)?

13.a) Consider the following snapshot of a system. Execute Banker's algorithm answer the following:

	Allocation	Max	Available
P_0	001	001	152
P_1	100	175	
P_2	135	235	
P_3	063	065	
P_4	001	065	

Is the system in a safe state? If the system is safe, show how all the process could complete the execution successfully. Explain.

OR

13.b) Explain the difference between external fragmentation and internal fragmentation? How to solve the fragmentation problem using paging?

14a) Explain the concept of demand paging in detail.

OR

14.b) Consider the following page – reference string:
2, 3, 4, 5, 3, 2, 6, 7, 3, 2, 3, 4, 1, 7, 1, 4, 3, 2, 3, 4, 7

Calculate the number of page faults would occur for the following page replacement algorithm with frame size of 3 and 5.
i) LRU ii) FIFO iii) Optimal

15 a) Explain the various allocation methods used in file systems.

OR

15.b) Explain the different disk scheduling algorithms with neat diagrams.

MODEL QUESTION PAPER # 2

V SEMESTER
CS1252 – OPERATING SYSTEMS

Time: Three Hours **Maximum : 100 Marks**

Answer All The Questions
PART – A (10 x 2 = 20 Marks)

1. Classify real time systems.
2. Processes call the operating system with system call interrupt instructions. Why can't processes make ordinary procedure calls to the operating systems?
3. What is meant by the context of a process?
4. Mention the methods for deadlock recovery in a system.
5. Consider the following set of processes, with the length of the CPU-burst time and the arrival time given in milliseconds:

Process	Arrival Time	Burst Time
P1	0	75
P2	10	40
P3	10	25
P4	80	20
P5	85	45

   a. Draw a Gantt chart illustrating the execution of these processes using preemptive SJF scheduling algorithm.
6. What is the relationship between program locality and TLB hit rate?
7. What is pre-paging?
8. What is thrashing?
9. Mention the advantages and disadvantages of continuous allocation of files.
10. List the main components of a Linux system.

PART-B 5x16 = 80 marks

11. a)(i) List and discuss the various services provided by the operating system.(8)

(ii) Write notes on Hardware protection. (8)

OR

11. b) i) In what ways is the modular kernel approach similar to the layered approach? In what ways does it differ from the layered approach? (4)

ii) How do clustered systems differ from multiprocessor systems? What is required for two machines belonging to a cluster to cooperate to provide a highly available service?(4)

iii) Compare batch operating system and time sharing operating system. (8)

12. (a) (i)Describe the actions taken by a kernel to context switch between kernel-level threads. (6)

(ii) Consider the following snapshot of a system:

	Allocation	Max	Available
	A B C D	A B C D	A B C D
P0	0 0 1 2	0 0 1 2	1 5 2 0
P1	1 0 0 0	1 7 5 0	
P2	1 3 5 4	2 3 5 6	
P3	0 6 3 2	0 6 5 2	
P4	0 0 1 4	0 6 5 6	

Answer the following questions using the banker's algorithm.

a. **What is the content of matrix Need? (4)**
b. **Is the system in a safe state? If yes, give the safe sequence.(2)**
c. **If a request from process P1 arrives for (0,4,2,0) can the request be granted immediately? (4)**

OR

12 b. (i) Given memory partitions of 100K, 500 K, 200 K, and 600K (in order), how would each of the First-fit, Best-fit, and Worst-fit algorithms place processes of 212K, 417K, 112K, and 426K (in order)? Which algorithm makes the most efficient use of memory? (10)

(ii) Why are segmentation and paging sometimes combined into one scheme? (6)

13. a. (i) Explain the Paged Memory Management Scheme. Indicate how the address translation is done. What are the advantages and disadvantages of this scheme? (10)

(ii) Discuss the hardware support required to support demand paging. (6)

OR

b) (i) How does a semaphore solve the critical section problem? Discuss whether semaphores satisfy the three requirements for a solution to the critical section problem. (8)

(ii) Explain the structure of a semaphore, wait and signal to overcome busy waiting.(8)

14. a. What is the cause of thrashing? Explain the methods by which thrashing could be controlled. (16)

OR

b. Describe different schemes for defining the logical structure of a directory. (16)

15. a. Discuss on the following disk scheduling algorithms:
Shortest Seek Time First, First Come First Served, SCAN, C- LOOK.(16)

OR

b. i) List and discuss the various methods for implementing a directory.(8)

ii) Some file systems allow disk storage to be allocated at different levels of granularity. For instance, a file system could allocate 4KB of disk space as a single 4 KB block or as 8 512 byte blocks. How could we take advantage of the flexibility to improve performance? What modifications would have to be made to the free-space management scheme in order to support this feature? (8)

MODEL QUESTION PAPER # 3
V SEMESTER
CS1252 – OPERATING SYSTEMS

Time: Three Hours **Maximum : 100 Marks**

Answer All The Questions

PART – A (10 x 2 = 20 Marks)

1. What is an Operating System?
2. What are the advantages of Multiprocessor Systems?
3. Name the various process states.
4. Define context switching.
5. Distinguish between pre emptive and non pre emptive scheduling.
6. What is TLB?
7. What is thrashing?
8. Mention the various file attributes.
9. What are the various free space management methods?

10. What are the various LINUX components?

PART – B (5 x 16 = 80 Marks)

11.a)i) Explain the features of real time system and time sharing system. (8)
ii) Explain how hardware protection is achieved? (8)

OR

11.b) i) state the purpose of short-term, medium-term, and long term schedules. Also discuss the differences among them. (6)
ii) List and discuss three general methods for passing parameters to the OS. (10)

12.i) Discuss in detail the various multithreading models.

OR

ii) Consider the following set of processes, with the length of the CPU-burst time given in milliseconds

Process	Burst Time
P1	10
P2	29
P3	3
P4	7
P5	12

The processes are assumed to have arrived in the order P1,P2,P3,P4,P5 all at time 0. Consider the FCFS, Non preemptive SJF, Round Robin (quantum = 10ms) scheduling algorithms. Illustrate the scheduling using Gantt Chart. Which algorithm will give the minimum average waiting time? Discuss.

13.a) Discuss in detail the solutions to the Critical-Section problem.

OR

13.b) Write short notes on :
i) Deadlock Avoidance
ii) Deadlock Detection

14.a) i)Give an example of an application that could benefit from operating system support for random access to indexed files.(4)
ii) List and briefly discuss the most common schemes for defining the logical structure of a directory (12)

OR

14.b) Explain how paging technique is implemented in memory.

15.a) Explain the various allocation methods used in file systems.

OR

15.b) Explain in detail about process scheduling in Linux systems.

---------- ALL THE BEST ----------

B.E/B.Tech. DEGREE EXAMINATION, APRIL/MAY 2008
CS 1252-OPERATING SYSTEMS

Answer all the questions.
PART A-(10X2=20 marks)

1. Specify the critical factor to be strictly followed in real time systems.
2. List out the three main advantages of multiprocessor system.
3. What is co-operating process?
4. What is bounded waiting in critical section?
5. What are the four necessary conditions a system should possess in order to be termed as deadlock?
6. What is segmentation?
7. Why should we use virtual memory?
8. What is meant by thrashing?
9. Name the entries that make up a File Control Block (FCB).
10. State any two distinguishing features of UNIX and Windows.

PART B (5 X 16=80 marks)

11.(a).(i).Explain the facilities by the following operating systems
(1).Clustered system and
(2).Real-Time system
(ii).List out the services provided by operating system to programs and to the user of the program.
(Or)
11.(b).(i).Explain the process creation and process termination process on process.
(ii).Write short notes on co-operating processors and schedulers.

12.(a)Describe the following scheduling algorithms
(i).Shortest job first scheduling
(ii).Round robin scheduling
(iii).Real time scheduling
(iv).Priority scheduling
(Or)
12.(b).What is the important feature of critical section? State the dining philosopher's problem and show how to allocate the several resources among several processors in a deadlock and starvation free manner.

13.(a).(i).How can deadlock be detected? Explain.
(ii).Write short notes on swapping.
(Or)

13.(b).Discuss the advantages of paging memory management and the conversion of logical address into physical address with necessary hardware.
14.(a).Discuss the following page replacement algorithms, giving a suitable page reference string (i).LRU (ii).FIFO and (iii).Optimal.
(Or)
14.(b).(i).State the various attributes of a file and their purpose. Discuss the various file operations.
(ii).Discuss about demand paging.

15.(a).Discuss in detail any three methods of implementing the file system.
(Or)
15.(b).Write short notes on:
(i).Disk structure
(ii).Indexed allocation
(iii).Shortest Seek Time First (SSTF) scheduling.

MODEL QUESTION PAPER # 4

Time: 3 hours Max. Marks: 100
Answer ALL Questions

PART-A 10x2 = 20 marks

1. Mention any two essential properties of real time systems.
2. Processes call the operating system with system call interrupt instructions. Why can't processes make ordinary procedure calls to the operating systems?
3. What is meant by the context of a process?
4. Mention the methods for deadlock recovery in a system.
5. Consider the following set of processes, with the length of the CPU-burst time and the arrival time given in milliseconds:

Process	Arrival Time	Burst Time
P1	0	75
P2	10	40

P3	10	25
P4	80	20
P5	85	45

a. Draw a Gantt chart illustrating the execution of these processes using preemptive SJF scheduling algorithm.

6. What is the relationship between program locality and TLB hit rate?
7. What is Belady's anomaly?
8. What is thrashing?
9. Mention the advantages and disadvantages of continuous allocation of files.
10. List the main components of a Linux system.

PART-B 5x16 = 80 marks

11. (i) Explain the MS-DOS system structure with a neat diagram. (8)
(ii) Write notes on Hardware protection. (8)

12. (a) (i)Describe the actions taken by a kernel to context switch between kernel-level threads. (4)
(ii) Consider the following snapshot of a system:

	Allocation	Max	Available
	A B C D	A B C D	A B C D
P0	0 0 1 2	0 0 1 2	1 5 2 0
P1	1 0 0 0	1 7 5 0	
P2	1 3 5 4	2 3 5 6	
P3	0 6 3 2	0 6 5 2	
P4	0 0 1 4	0 6 5 6	

Answer the following questions using the banker's algorithm.

a. What is the content of matrix Need? (2)
b. Is the system in a safe state? If yes, give the safe sequence. (2)
c. If a request from process P1 arrives for (0,4,2,0) can the request be granted immediately? (4)

(iii)Distinguish between short term, long term and medium term scheduling.(4)

OR
b) (i) How does a semaphore solve the critical section problem? Discuss whether semaphores satisfy the three requirements for a solution to the critical section problem. (8)
(ii) A barbershop consists of a waiting room with n chairs and the barber room containing the barber chair. If there are no customers to be served, the barber goes to sleep. If a

customer enters the barbershop and all chairs are occupied, then the customer leaves the shop. If the barber is busy but chairs are available, then the customer sits in one of the free chairs. If the barber is asleep, the customer wakes up the barber. Write a program to coordinate the barber and the customers. (8)

13. a. (i) Given memory partitions of 100K, 500 K, 200 K, and 600K (in order), how would each of the First-fit, Best-fit, and Worst-fit algorithms place processes of 212K, 417K, 112K, and 426K (in order)? Which algorithm makes the most efficient use of memory? (8)

(ii) Write down the different issues in real time scheduling. (8)

OR

b. (i) Explain segmentation with a neat diagram. (8)

(ii) Consider a variation of round-robin we will call progressive round-robin. In progressive round-robin, each process has its own time quantum. This starts out at 50 ms, and increases by 50 ms each time it goes through the round-robin queue. Give the advantages and disadvantages of this variant over ordinary round-robin. (8)

14. a. What is the cause of thrashing? Explain the methods by which thrashing could be controlled. (16)

OR

b. Describe different schemes for defining the logical structure of a directory. (16)

15. a. Discuss on the following disk scheduling algorithms:
Shortest Seek Time First, First Come First Served, SCAN, and C- LOOK.
(16)

OR

b. Explain briefly how process management is done in Linux. (16)

B.E/B.Tech.DEGREE EXAMINATION,NOVEMBER/DECEMBER 2004.
CS1252 – OPERATING SYSTEMS

Time: Three hours Maximum:100 marks

Answer ALL questions

PART A – (10* 2= 20 marks)

1. What is Time Sharing System?

2. What is the main advantage of the layered approach to system design.

3. What is job scheduler? What is CPU scheduler?

4. What are the various process states?Depict process state diagram.

5. Explain any four scheduling criteria involved in CPU scheduling.

6. Consider a logical address space of eight pages of 1024 words each, mapped onto a physical memory of 32 Frames. How many bits are there in logical address?

7. What is sequential address method? Mention its merits and demerits.

8. Define single level directory structure. Give one example.

9. What is a bit vector?

10. Mention any two features of linux file system.

PART B - (5 * 16 = 80 marks)

11. (i) Describe Working-Set model. (10)

(ii) Describe paging with illustrative example. (6)

12. (a) (i) Consider the following set of processes , with the length of the CPU burst time given in milliseconds.

Process	Burst time	Priority
P1	8	3
P2	3	1
P3	4	4
P4	2	2
P5	6	5

The processes are assumed to have arrived in the order P1, P2, P3, P4 and P5 all at time 'O'.

(1) Draw four Gantt charts illustrating the execution of these processes using FCFS, SJF, A nonpreemptive priority (a smaller priority number implies a higher priority) and RR (quantum = 2) scheduling.

(2) What is the turn around time of each process for each of the scheduling algorithms in part (1).

(3) What is the waiting time of each process for each of the

scheduling algorithms in part (1).

(4) Which of the schedules in part (1) results in the minimal average waiting time(over all processes) (12)

(ii) Explain the three requirements that a solution to critical-section problem must satisfy. (4)

Or

(b) (i) Describe an algorithm which satisfies all the conditions of critical section problem and also prove how it satisfies all the conditions. (6)

(ii) Describe deadlock prevention methods

(1) Hold and wait

(2) Circular wait

(3) No preemption. (10)

13. (a) (i) Describe internal and external fragmentation with illustrative examples. (8)

(ii) Describe segmentation with its hardware. (8)

Or

(b) (i) Describe multilevel paging with example. (8)

(ii) Describe hardware support of paging with TLB. (8)

14. (a) Describe place replacement algorithms

(i) FIFO algorithm

(ii) Optimal algorithm

(iii) LRU algorithm with illustrative example. (16)

Or

(b) (i) Describe the layered design of file-system organization. (10)

(ii) Describe the file system mounting. (6)

15. (a) Describe the following methods for allocating disk space.

(i) Linked allocation.

(ii) Contiguous allocation. (16)

Or

(b) (i) Describe components of a Linux system. (8)

(ii) Describe process scheduling in Linux system. (8)

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2009.

Fifth Semester

Information Technology

CS1252 – OPERATING SYSTEMS

Time: Three hours **Maximum: 100 marks**

Answer ALL questions.

PART A – (10 X 2 = 20 MARKS)

1. Write pros and cons of Hard Real time system and Soft Real Time system.
2. What are cooperating processes? Give an example.
3. State the resources that are used when a thread is created? How do they differ from those used when a process is created?
4. State why a swapping scheme is implemented in a medium term scheduler.
5. Mention the necessary conditions for Deadlock occurrence.
6. If a computer system has 16-bit address line and supports 1 K page size, what will be the maximum page number supported by this system.
7. How does the system detect thrashing? Briefly state.
8. What are immutable shared files?
9. State the major goal for the design and implementation of swap space.
10. List the components of on-disk structure of file system.

PART B - (5 X 16 = 80 MARKS)

11. (a) Explain the message passing inter processes communication and the various methods for logically implementing them. (16)

Or

(b) (i) What is the need for system calls? How system calls are used? Explain with an example. (10)

(ii) Explain the process state diagram. (6)

12. (a) (i) Write the "C" implementation of semaphores and the operations on it.

(ii) Define the critical section problem and discuss the three requirements that a solution to the critical section problem must satisfy. (8)

Or

(b) (i) What are the advantages of threads? Describe the multi-threaded models.(8)

(ii) What is the advantage of having different time-quantum sizes at different levels Multi-level Feedback Queue (MFQ) based scheduling? (8)

13. (a) Explain the difference between External Fragmentation and Internal Fragmentation. How to solve the fragmentation problem using paging? (6+10)

Or

(b) (i) Explain Banker's algorithm for deadlock avoidance. (8)

(ii) With relevant diagrams and examples discuss the advantages and disadvantages of continuous memory allocation schemes. (8)

14. (a) What are the causes of thrashing? Explain working-set model with an example.

(16)

Or

(b) Consider the following page reference string:

1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6.

How many page faults would occur for the following replacement algorithms, assuming one, two, three and four frames?

(i) LRU replacement

(ii) FIFO replacement

(iii) Optimal replacement

Remember that all frames are initially empty, so your first unique pages will all cost one fault each. (16)

15. (a) (i) Explain the linked allocation and indexed allocation methods used in file systems. (8)

(ii) Compare and contrast “free-space management” and “swap space management”. (8)

Or

(b) Discuss the various techniques through which files can be allocated space on disk. Give relevant example and diagrammatic illustration. (16)

ALL THE BEST

IT 2251 SOFTWARE ENGINEERING AND QUALITY ASSURANCE

SYLLABUS

1. Software Product And Process **9**

Introduction – S/W Engineering Paradigm – Verification – Validation – Life Cycle Models – System Engineering – Computer Based System – Business Process Engineering Overview – Product Engineering Overview.

2. Software Requirements **9**

Functional and Non-Functional – Software Document – Requirement Engineering Process – Feasibility Studies – Software Prototyping – Prototyping in the Software Process – Data – Functional and Behavioral Models – Structured Analysis and Data Dictionary.

3. Analysis, Design Concepts And Principles **9**

Systems Engineering - Analysis Concepts - Design Process And Concepts – Modular Design – Design Heuristic – Architectural Design – Data Design – User Interface Design – Real Time Software Design – System Design – Real Time Executives – Data Acquisition System – Monitoring And Control System.

4. Testing **9**

Taxonomy Of Software Testing – Types Of S/W Test – Black Box Testing – Testing Boundary Conditions – Structural Testing – Test Coverage Criteria Based On Data Flow Mechanisms – Regression Testing – Unit Testing – Integration Testing – Validation Testing – System Testing And Debugging – Software Implementation Techniques

5. Software Quality Assurance 9

Process and Product Quality – Quality Assurance and Standards – Quality Planning and Control – Software metrics – Process Improvement – Software configuration Management.

TOTAL = 45

TEXT BOOKS:

1. Ian Sommerville, “Software engineering”, Seventh Edition, Pearson Education Asia, 2007.
2. Roger S. Pressman, “Software Engineering – A practitioner’s Approach”, Sixth Edition, McGraw-Hill International Edition, 2005.

REFERENCES:

1. Watts S.Humphrey,”A Discipline for Software Engineering”, Pearson Education, 2007.
2. James F.Peters and Witold Pedrycz,”Software Engineering, An Engineering Approach”, Wiley-India, 2007.
3. Stephen R.Schach, “ Software Engineering”, Tata McGraw-Hill Publishing Company Limited, 2007.
4. S.A.Kelkar,”Software Engineering”, Prentice Hall of India Pvt, 2007.

TWO MARKS

UNIT 1

1. **What is software engineering?**
Software engineering is a discipline in which theories, methods and tools are applied to develop professional software.

2. What is Software ?
Software is nothing but a collection of computer programs that are related documents that are indented to provide desired features, functionalities and better performance.

3. What are the characteristics of the software?
- Software is engineered, not manufactured.
- Software does not wear out.
- Most software is custom built rather than being assembled from components.

4. **What are the various categories of software?**
- System software Application
- software Engineering/Scientific software
- Embedded software
- Web Applications
- Artificial Intelligence software

5. **What are the challenges in software?**
- Copying with legacy systems.
- Heterogeneity challenge
- Delivery times challenge

6. **Define software process**.
Software process is defined as the structured set of activities that are required to develop the software system.

7. What are the fundamental activities of a software process?
- Specification
- Design and implementation
- Validation
- Evolution

8. What are the umbrella activities of a software process?
- Software project tracking and control.
- Risk management.
- Software Quality Assurance.
- Formal Technical Reviews.
- Software Configuration Management.
- Work product preparation and production.
- Reusability management. Measurement.

9. What are the merits of incremental model?
i. The incremental model can be adopted when there are less number of people involved in the project.
ii. Technical risks can be managed with each increment.
iii. For a very small time span, at least core product can be delivered to the customer.

10. List the task regions in the Spiral model.
Customer communication – In this region it is suggested to establish customer communication.
Planning – All planning activities are carried out in order to define resources timeline and other project related activities.
Risk analysis – The tasks required to calculate technical and management risks.
Engineering – In this the task region, tasks required to build one or more representations of applications are carried out.
Construct and release – All the necessary tasks required to construct, test, install the applications are conducted.
Customer evaluation – Customer's feedback is obtained and based on the customer evaluation required tasks are performed and implemented at installation stage.

11. What are the drawbacks of spiral model?
i. It is based on customer communication.If the communication is not proper then the software product that gets developed will not be the up to the mark.
ii. It demands considerable risk assessment.If the risk assessment is done properly then only the successful product can be obtained.

12. What is System Engineering?
System Engineering means designing, implementing, deploying and operating systems which include hardware, software and people.

13**. List the process maturity levels in SEIs CMM.**
Level 1:Initial – Few processes are defined and individual efforts are taken.
Level 2:Repeatable – To track cost schedule and functionality basic project management processes are established.
Level 3:Defined – The process is standardized, documented and followed.
Level 4:Managed – Both the software process and product are quantitatively understood and controlled using detailed measures.
Level 5:Optimizing – Establish mechanisms to plan and implement change.

14. **What is an effector process?**
The effector process is a process that verifies itself.The effector process exists in certain criteria.

15. Define the computer based system.
The computer based system can be defined as "a set or an arrangement of elements that are organized to accomplish some predefined goal by processing information".

16. What does Verification represent?
Verification represents the set of activities that are carried out to confirm that the software correctly implements the specific functionality.

17. What does Validation represent?
Validation represents the set of activities that ensure that the software that has been built is satisfying the customer requirements.

18. What are the steps followed in testing?
i. **Unit testing –** The individual components are tested in this type of testing.
ii. Module testing – Related collection of independent components are tested.
iii. Sub-system testing – This is a kind of integration testing.Various modules are integrated into a subsystem and the whole subsystem is tested.
iv. System testing – The whole system is tested in this system.
v. **Acceptance testing –** This type of testing involves testing of the system with customer data.If the system behaves as per customer need then it is accepted.

19. What is the use of CMM?
Capability Maturity Model is used in assessing how well an organisation's processes allow to complete and manage new software projects.

20. Name the Evolutionary process Models.
i. Incremental model
ii. Spiral model
iii. WIN-WIN spiral model
iv. Concurrent Development

UNIT 2:

21. What is requirement engineering?
Requirement engineering is the process of establishing the services that the customer requires from the system and the constraints under which it operates and is developed.

22. What are the various types of traceability in software engineering?
i. Source traceability – These are basically the links from requirement to stakeholders who propose these requirements.
ii. Requirements traceability – These are links between dependant requirements.
iii. **Design traceability –** These are links from requirements to design.

23. Define software prototyping.
Software prototyping is defined as a rapid software development for validating the requirements.

24. What are the benefits of prototyping?
i. Prototype serves as a basis for deriving system specification.
ii. Design quality can be improved.
iii. System can be maintained easily.
iv. Development efforts may get reduced.
v. System usability can be improved.

25. What are the prototyping approaches in software process?
i. Evolutionary prototyping – In this approach of system development, the initial prototype is prepared and it is then refined through number of stages to final stage.
ii. **Throw-away prototyping –** Using this approach a rough practical implementation of the system is produced. The requirement problems can be identified from this implementation. It is then discarded. System is then developed using some different engineering paradigm.

26. What are the advantages of evolutionary prototyping?
i. Fast delivery of the working system.
ii. User is involved while developing the system.
iii. More useful system can be delivered.
iv. Specification,design and implementation work in co-ordinated manner.

27. What are the various Rapid prototyping techniques?
i. Dynamic high level language development.
ii. Database programming.
iii. Component and application assembly.

28. What is the use of User Interface prototyping?
This prototyping is used to pre-specify the look and feel of user interface in an effective way.

29. What are the characteristics of SRS?
i. Correct – The SRS should be made up to date when appropriate requirements are identified.
ii. Unambiguous – When the requirements are correctly understood then only it is possible to write an unambiguous software.
iii. Complete – To make SRS complete, it should be specified what a software designer wants to create software.
iv. Consistent – It should be consistent with reference to the functionalities identified.
v. Specific – The requirements should be mentioned specifically.
vi. **Traceable –** What is the need for mentioned requirement? This should be correctly identified.

30. What are the objectives of Analysis modeling?
i. To describe what the customer requires.
ii. To establish a basis for the creation of software design.
iii. To devise a set of valid requirements after which the software can be built.

31. What is data modeling?
Data modeling is the basic step in the analysis modeling. In data modeling the data objects are examined independently of processing. The data model represents how data are related with one another.
32. What is a data object?
Data object is a collection of attributes that act as an aspect, characteristic, quality, or descriptor of the object.

33. What are attributes?
Attributes are the one, which defines the properties of data object.

34. What is cardinality in data modeling?
Cardinality in data modeling, cardinality specifies how the number of occurrences of one object is related to the number of occurrences of another object.

35. What does modality in data modeling indicates?
Modality indicates whether or not a particular data object must participate in the relationship.

36. What is ERD?
Entity Relationship Diagram is the graphical representation of the object relationship pair. It is mainly used in database applications.

37. What is DFD?
Data Flow Diagram depicts the information flow and the transforms that are applied on the data as it moves from input to output.

38. What does Level0 DFD represent?

Level0 DFD is called as ‘fundamental system model’ or ‘context model’. In the context model the entire software system is represented by a single bubble with input and output indicated by incoming and outgoing arrows.

39. What is a state transition diagram?
State transition diagram is basically a collection of states and events. The events cause the system to change its state. It also represents what actions are to be taken on the occurrence of particular event.

40. **Define Data Dictionary**.
The data dictionary can be defined as an organized collection of all the data elements of the system with precise and rigorous definitions so that user and system analyst will have a common understanding of inputs, outputs, components of stores and intermediate calculations.

41. What are the elements of Analysis model?
i. Data Dictionary
ii. Entity Relationship Diagram
iii. Data Flow Diagram
iv. State Transition Diagram
v. Control Specification
vi. Process specification

UNIT 3:

42. What are the elements of design model?
i. Data design
ii. Architectural design
iii. Interface design
iv. Component-level design

43. Define design process.
Design process is a sequence of steps carried through which the requirements are translated into a system or software model.

44. List the principles of a software design.
i. The design process should not suffer from "tunnel vision".
ii. The design should be traceable to the analysis model.
iii. The design should exhibit uniformity and integration.
iv. Design is not coding.
v. The design should not reinvent the wheel.

45. What is the benefit of modular design?
Changes made during testing and maintenance becomes manageable and they do not affect other modules.

46. What is a cohesive module?
A cohesive module performs only "one task" in software procedure with little interaction with other modules. In other words cohesive module performs only one thing.

47. What are the different types of Cohesion?
i. Coincidentally cohesive –The modules in which the set I\of tasks are related with each other loosely then such modules are called coincidentally cohesive.
ii. Logically cohesive – A module that performs the tasks that are logically related with each other is called logically cohesive.
iii. Temporal cohesion – The module in which the tasks need to be executed in some specific time span is called temporal cohesive.
iv. Procedural cohesion – When processing elements of a module are related with one another and must be executed in some specific order then such module is called procedural cohesive.
v. **Communicational cohesion –** When the processing elements of a module share the data then such module is called communicational cohesive.

48. What is Coupling?
Coupling is the measure of interconnection among modules in a program structure. It depends on the interface complexity between modules.

49. What are the various types of coupling?

i. Data coupling – The data coupling is possible by parameter passing or data interaction.
ii. Control coupling – The modules share related control data in control coupling.
iii. Common coupling – The common data or a global data is shared among modules.
iv. **Content coupling** – Content coupling occurs when one module makes use of data or control information maintained in another module.

50. What are the common activities in design process?
i. **System structuring** – The system is subdivided into principle subsystems components and communications between these subsystems are identified.
ii. **Control modeling –** A model of control relationships between different parts of the system is established.
iii. Modular decomposition – The identified subsystems are decomposed into modules.

51. What are the benefits of horizontal partitioning?
i. Software that is easy to test.
ii. Software that is easier to maintain.
iii. Propagation of fewer side effects.
iv. Software that is easier to extend.

52. What is vertical partitioning?
Vertical partitioning often called factoring suggests that the control and work should be distributed top-down in program structure.

53. What are the advantages of vertical partitioning?
i. These are easy to maintain changes.
ii. They reduce the change impact and error propagation.

54. What are the various elements of data design?
i. Data object – The data objects are identified and relationship among various data objects can be represented using ERD or data dictionaries.
ii. **Databases –** Using software design model, the data models are translated into data structures and data bases at the application level.
iii. **Data warehouses –** At the business level useful information is identified from various databases and the data warehouses are created.

55. List the guidelines for data design.
i. Apply systematic analysis on data.
ii. Identify data structures and related operations.
iii. Establish data dictionary.
iv. Use information hiding in the design of data structure.
v. Apply a library of useful data structures and operations.

56. Name the commonly used architectural styles.
i. Data centered architecture.
ii. Data flow architecture.
iii. Call and return architecture.

iv. Object-oriented architecture.
v. Layered architecture.

57. What is Transform mapping?
The transform mapping is a set of design steps applied on the DFD in order to map the transformed flow characteristics into specific architectural style.

58. What is a Real time system?
Real time system is a software system in which the correct functionalities of the system are dependent upon results produced by the system and the time at which these results are produced.

59. What is SCM?
Software Configuration Management is a set of activities carried out for identifying, organizing and controlling changes throughout the lifecycle of computer software.

60. What is SCI?
Software Configuration Item is information that is carried as part of the software engineering process.

UNIT 4:

61. Define software testing?
Software testing is a critical element of software quality assurance and represents the ultimate review of specification, design, and coding.

62. What are the objectives of testing?
i. Testing is a process of executing a program with the intend of finding an error.
ii. A good test case is one that has high probability of finding an undiscovered error.
iii. A successful test is one that uncovers as an-yet undiscovered error.

63. **What are the testing principles the software engineer must apply while performing the software testing?**
i. All tests should be traceable to customer requirements.
ii. Tests should be planned long before testing begins.
iii. The pareto principle can be applied to software testing-80% of all errors uncovered during testing will likely be traceable to 20% of all program modules.
iv. Testing should begin "in the small" and progress toward testing "in the large".
v. Exhaustive testing is not possible.
vi. To be most effective, an independent third party should conduct testing.

63. What are the two levels of testing?
i. Component testing
Individual components are tested. Tests are derived from developer' s experience.
ii. System Testing
The group of components is integrated to create a system or sub-system is done. These tests are based on the system specification.

64. What are the various testing activities?
i. Test planning
ii. Test case design
iii. Test execution
iv. Data collection
v. Effective evaluation

65. Write short note on black box testing.
The black box testing is also called as behavioral testing. This method fully focus on the functional requirements of the software. Tests are derived that fully exercise all functional requirements.

66. What is equivalence partitioning?
Equivalence partitioning is a black box technique that divides the input domain into classes of data. From this data test cases can be derived. Equivalence class represents a set of valid or invalid states for input conditions.

67. What is a boundary value analysis?
A boundary value analysis is a testing technique in which the elements at the edge of the domain are selected and tested. It is a test case design technique that complements equivalence partitioning technique. Here instead of focusing on input conditions only, the test cases are derived from the output domain.

68. What are the reasons behind to perform white box testing?
There are three main reasons behind performing the white box testing.
1. Programmers may have some incorrect assumptions while designing or implementing some functions.Due to this there are chances of having logical errors in the program.To detect and correct such logical errors procedural details need to be examined.
2. Certain assumptions on flow of control and data may lead programmer to make design errors. To uncover the errors on logical path, white box testing is must.
3. There may be certain typographical errors that remain undetected even after syntax and type checking mechanisms. Such errors can be uncovered during white box testing.

69. What is cyclomatic complexity?
Cyclomatic complexity is a software metric that gives the quantitative measure of logical complexity of the program.
The Cyclomatic complexity defines the number of independent paths in the basis set of the program that provides the upper bound for the number of tests that must be conducted to ensure that all the statements have been executed at least once.

70. How to compute the cyclomatic complexity?
The cyclomatic complexity can be computed by any one of the following ways.
1. The numbers of regions of the flow graph correspond to the cyclomatic complexity.
2. Cyclomatic complexity,V(G),for the flow graph,G,is defined as: V(G)=E-N+2,
E -- number of flow graph edges,
N -- number of flow graph nodes
3. V(G)=P+1
Where P is the number of predicate nodes contained in the flow graph.

71. Distinguish between verification and validation.
Verification refers to the set of activities that ensure that software correctly implements a specific function. **Validation** refers to a different set of activities that ensure that the software that has been built is traceable to the customer requirements.
According to Boehm, **Verification**:" Are we building the product right?" Validation:" Are we building the right product?"

72. What are the various testing strategies for conventional software?
i. Unit testing
ii. Integration testing.
iii. Validation testing.
iv. System testing.

73. Write about drivers and stubs.
Drivers and stub software need to be developed to test incompatible software.

- The " **driver**" is a program that accepts the test data and prints the
- relevant results.
- The " **stub**" is a subprogram that uses the module interfaces and performs the minimal data manipulation if required.

74. What are the approaches of integration testing?
The integration testing can be carried out using two approaches.
1. The non-incremental testing.
2. Incremental testing.

75. What are the advantages and disadvantages of big-bang?
Advantages: This approach is simple.
Disadvantages: It is hard to debug. It is not easy to isolate errors while testing. In this approach it is not easy to validate test results. After performing testing, it is impossible to form an integrated system.

76. What are the benefits of smoke testing?
- Integration risk is minimized.
- The quality of the end-product is improved.
- Error diagnosis and correction are simplified.
- Assessment of program is easy.

77. What are the conditions exists after performing validation testing?
After performing the validation testing there exists two conditions.
- The function or performance characteristics are according to the specifications and are accepted.
- The requirement specifications are derived and the deficiency list is created.
- The deficiencies then can be resolved by establishing the proper communication with the customer.

78. **Distinguish between alpha and beta testing**.
Alpha and beta testing are the types of acceptance testing.
Alpha test: The alpha testing is attesting in which the version of complete software is tested by the customer under the supervision of developer. This testing is performed at developer' s site.
Beta test: The beta testing is a testing in which the version of the software is tested by the customer without the developer being present. This testing is performed at customer' s site.

79. What are the various types of system testing?
1. **Recovery testing** – is intended to check the system' s ability to recover from failures.
2. **Security testing –** verifies that system protection mechanism prevent improper penetration or data alteration.
3. **Stress testing –** Determines breakpoint of a system to establish maximum service level.

4**. Performance testing –** evaluates the run time performance of the software, especially real-time software.

80. Define debugging.
Debugging is defined as the process of removal of defect. It occurs as a consequence of successful testing.

81. What are the common approaches in debugging?
Brute force method: The memory dumps and run-time tracks are examined and program with write statements is loaded to obtain clues to error causes.
Back tracking method: The source code is examined by looking backwards from symptom to potential causes of errors.
Cause elimination method: This method uses binary partitioning to reduce the number of locations where errors can exists.

82. What are the metrics computed during error tracking activity? Errors per requirement specification page. Errors per component-design level Errors per component-code level DRE-requirement analysis DRE-architectural analysis DRE-component level design DRE-coding.

UNIT 5:

83. What is quality?
- Quality, simplistically, means that a product should meet its specification.
- This is problematical for software systems
- There is a tension between customer quality requirements (efficiency, reliability, etc.) and developer quality requirements (maintainability, reusability, etc.);
- Some quality requirements are difficult to specify in an unambiguous way;
- Software specifications are usually incomplete and often inconsistent.

84. What are Quality management activities.
- Quality assurance
  - Establish organisational procedures and standards for quality.
- Quality planning
  - Select applicable procedures and standards for a particular project and modify these as required.
- Quality control
  - Ensure that procedures and standards are followed by the software development team.
- Quality management should be separate from project management to ensure independence.

85.What is Process and product quality?
- The quality of a developed product is influenced by the quality of the production process.
- This is important in software development as some product quality attributes are hard to assess.
- However, there is a very complex and poorly understood relationship between software processes and product quality.

86.what is Quality assurance and standards?
- Standards are the key to effective quality management.
- They may be international, national, organizational or project standards.
- Product standards define characteristics that all components should exhibit e.g. a common programming style.
- Process standards define how the software process should be enacted.

87.Write the Importance of standards.
- Encapsulation of best practice- avoids repetition of past mistakes.
- They are a framework for quality assurance processes - they involve checking compliance to standards.
- They provide continuity - new staff can understand the organisation by understanding the standards that are used.

88.what is ISO 9000 certification?
- Quality standards and procedures should be documented in an organisational quality manual.

●An external body may certify that an organisation's quality manual conforms to ISO 9000 standards.
●Some customers require suppliers to be ISO 9000 certified although the need for flexibility here is increasingly recognised.

89.What is Documentation standards?
●Particularly important - documents are the tangible manifestation of the software.
●Documentation process standards
•Concerned with how documents should be developed, validated and maintained.
●Document standards
•Concerned with document contents, structure, and appearance.
●Document interchange standards
•Concerned with the compatibility of electronic documents.

90. What is Quality plans?
●Quality plan structure
•Product introduction;
•Product plans;
•Process descriptions;
•Quality goals;
•Risks and risk management.
●Quality plans should be short, succinct documents
•If they are too long, no-one will read them.

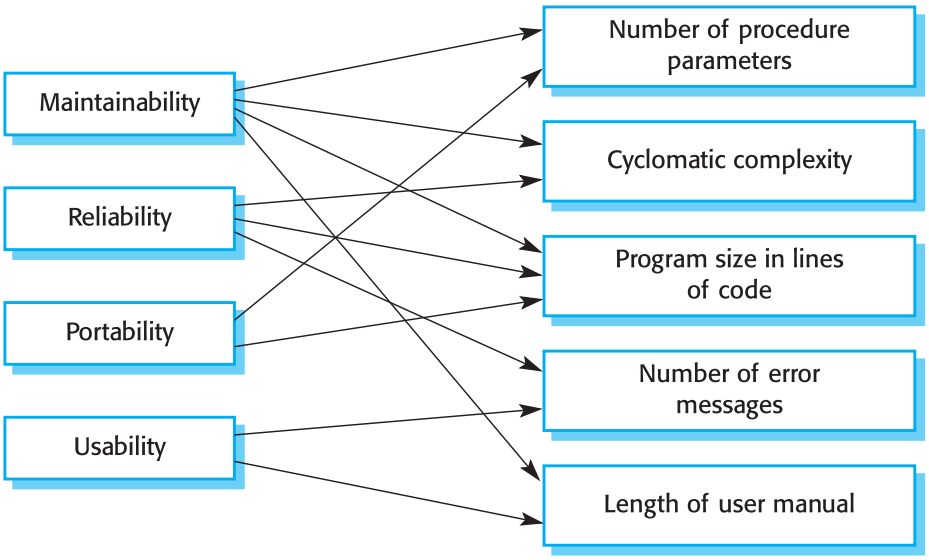
91.What is Quality control?
●This involves checking the software development process to ensure that procedures and standards are being followed.
●There are two approaches to quality control
•Quality reviews;
•Automated software assessment and software measurement.

92.What is Quality reviews?
●This is the principal method of validating the quality of a process or of a product.
●A group examines part or all of a process or system and its documentation to find potential problems.
●There are different types of review with different objectives
•Inspections for defect removal (product);
•Reviews for progress assessment (product and process);
•Quality reviews (product and standards).

93. What is Software metric?
●Any type of measurement which relates to a software system, process or related documentation
•Lines of code in a program, the Fog index, number of person-days required to develop a component.
●Allow the software and the software process to be quantified.

•May be used to predict product attributes or to control the software process.
•Product metrics can be used for general predictions or to identify anomalous components.

94.What is Internal and external attributes?



95. What is Product metrics?
•A quality metric should be a predictor of product quality.
•Classes of product metric
•Dynamic metrics which are collected by measurements made of a program in execution;
•Static metrics which are collected by measurements made of the system representations;
•Dynamic metrics help assess efficiency and reliability; static metrics help assess complexity, understandability and maintainability.

96.What is Dynamic and static metrics?
•Dynamic metrics are closely related to software quality attributes
•It is relatively easy to measure the response time of a system (performance attribute) or the number of failures (reliability attribute).
•Static metrics have an indirect relationship with quality attributes
•You need to try and derive a relationship between these metrics and properties such as complexity, understandability and maintainability.

97.What is Process improvement?

- Understanding existing processes and introducing process changes to improve product quality, reduce costs or accelerate schedules.
- Most process improvement work so far has focused on defect reduction. This reflects the increasing attention paid by industry to quality.
- However, other process attributes can also be the focus of improvement

98.What is Quality factors?

- For large projects with 'average' capabilities, the development process determines product quality.
- For small projects, the capabilities of the developers is the main determinant.
- The development technology is particularly significant for small projects.
- In all cases, if an unrealistic schedule is imposed then product quality will suffer.

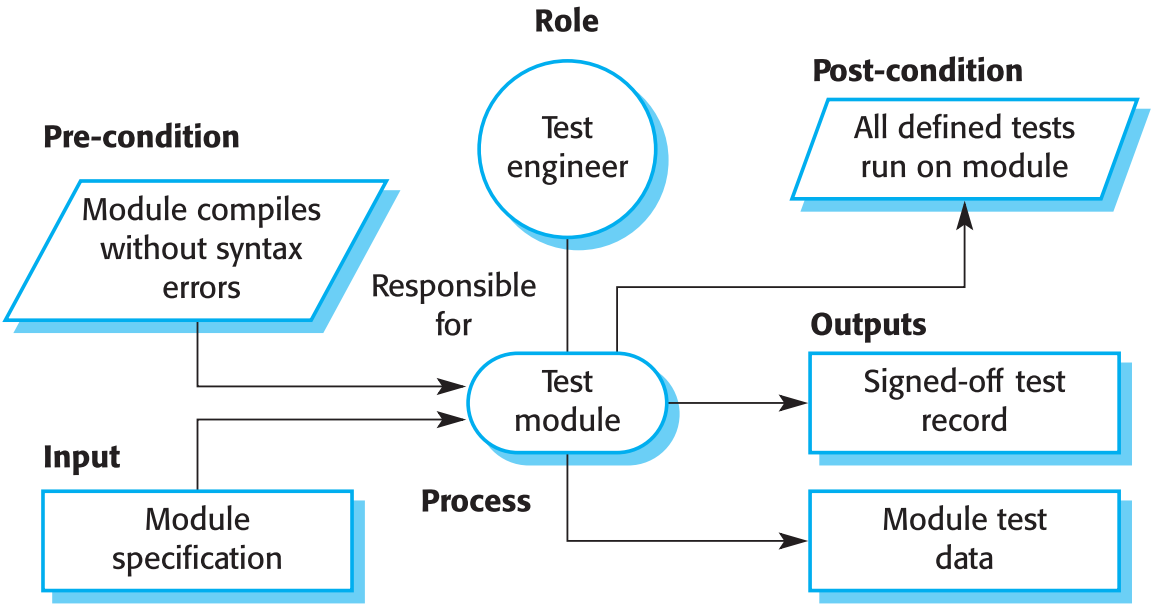
99.Write the Process classification.

- Informal
  - No detailed process model. Development team chose their own way of working.
- Managed
  - Defined process model which drives the development process.
- Methodical
  - Processes supported by some development method such as the RUP.
- Supported
  - Processes supported by automated CASE tools.

100. What is Process analysis and modelling?

- Process analysis
  - The study of existing processes to understand the relationships between parts of the process and to compare them with other processes.
- Process modelling
  - The documentation of a process which records the tasks, the roles and the entities used;
  - Process models may be presented from different perspectives.

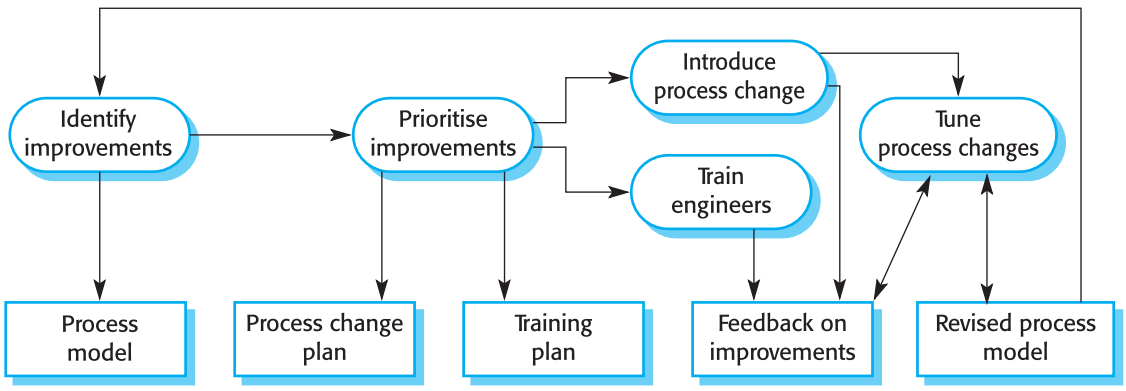
101.Draw the module testing activity.



102. What is Process change
- Involves making modifications to existing processes.
- This may involve:
- Introducing new practices, methods or processes;
- Changing the ordering of process activities;
- Introducing or removing deliverables;
- Introducing new roles or responsibilities.
- Change should be driven by measurable goals.

103.What are Process change stages?
- Improvement identification.
- Improvement prioritisation.
- Process change introduction.
- Process change training.
- Change tuning.

104. What is process change process?



105.What is CMMI framework?

- The CMMI framework is the current stage of work on process assessment and improvement that started at the Software Engineering Institute in the 1980s.
- The SEI's mission is to promote software technology transfer particularly to US defence contractors.
- It has had a profound influence on process improvement

•Capability Maturity Model introduced in the early 1990s.
•Revised maturity framework (CMMI) introduced in 2001.

106.What is SEI capability maturity model?

- Initial

•Essentially uncontrolled

- Repeatable

•Product management procedures defined and used

- Defined

•Process management procedures and strategies defined and used

- Managed

•Quality management strategies defined and used

- Optimising

•Process improvement strategies defined and used

107. What are CMMI model components?

- Process areas

•24 process areas that are relevant to process capability and improvement are identified. These are organised into 4 groups.

- Goals

•Goals are descriptions of desirable organisational states. Each process area has associated goals.

- Practices

•Practices are ways of achieving a goal - however, they are advisory and other approaches to achieve the goal may be used.

108. What is CMMI assessment?

- Examines the processes used in an organisation and assesses their maturity in each process area.
- Based on a 6-point scale:

•Not performed;
•Performed;
•Managed;
•Defined;
•Quantitatively managed;
•Optimizing.

109. What is continuous CMMI model

- This is a finer-grain model that considers individual or groups of practices and assesses their use.
- The maturity assessment is not a single value but is a set of values showing the organisations maturity in each area.
- The CMMI rates each process area from levels 1 to 5.
- The advantage of a continuous approach is that organisations can pick and choose process areas to improve according to their local needs.

110.Write the Problems with the CMM.

- Practices associated with model levels
  - Companies could be using practices from different levels at the same time but if all practices from a lower level were not used, it was not possible to move beyond that level
- Discrete rather than continuous
  - Did not recognise distinctions between the top and the bottom of levels
- Practice-oriented
  - Concerned with how things were done (the practices) rather than the goals to be achieved.

111. What is SCM?

Software Configuration Management is a set of activities carried out for identifying, organizing and controlling changes throughout the lifecycle of computer software.

112. What is SCI?

Software Configuration Item is information that is carried as part of the software engineering process.

113.What is Configuration management planning?

- All products of the software process may have to be managed:
  - Specifications;
  - Designs;
  - Programs;
  - Test data;
  - User manuals.
- Thousands of separate documents may be generated for a large, complex software system.

114. What is CM plan?

- Defines the types of documents to be managed and a document naming scheme.
- Defines who takes responsibility for the CM procedures and creation of baselines.
- Defines policies for change control and version management.
- Defines the CM records which must be maintained.
- Describes the tools which should be used to assist the CM process and any limitations on their use.
- Defines the process of tool use.
- Defines the CM database used to record configuration information.

●May include information such as the CM of external software, process auditing, etc.

115. What is Change management?
●Software systems are subject to continual change requests;
•From users;
•From developers;
•From market forces.
●Change management is concerned with keeping track of these changes and ensuring that they are implemented in the most cost-effective way.

116. What is Version and release management?
●Invent an identification scheme for system versions.
●Plan when a new system version is to be produced.
●Ensure that version management procedures and tools are properly applied.
●Plan and distribute new system releases.

117. What is Versions/variants/releases?
●Version An instance of a system which is functionally distinct in some way from other system instances.
●Variant An instance of a system which is functionally identical but non-functionally distinct from other instances of a system.
●Release An instance of a system which is distributed to users outside of the development team.
118.Use of CASE tools in configuration management
●CM processes are standardised and involve applying pre-defined procedures.
●Large amounts of data must be managed.
●CASE tool support for CM is therefore essential.
●Mature CASE tools to support configuration management are available ranging from stand-alone tools to integrated CM workbenches.

119.What is Change management tools?
●Change management is a procedural process so it can be modelled and integrated with a version management system.
●Change management tools
•Form editor to support processing the change request forms;
•Workflow system to define who does what and to automate information transfer;
•Change database that manages change proposals and is linked to a VM system;
•Change reporting system that generates management reports on the status of change requests.

120.What is Version management tools?
●Version and release identification
•Systems assign identifiers automatically when a new version is submitted to the system.
●Storage management.
•System stores the differences between versions rather than all the version code.
●Change history recording

- Record reasons for version creation.
- Independent development
- Only one version at a time may be checked out for change. Parallel working on different versions.
- Project support
- Can manage groups of files associated with a project rather than just single files.

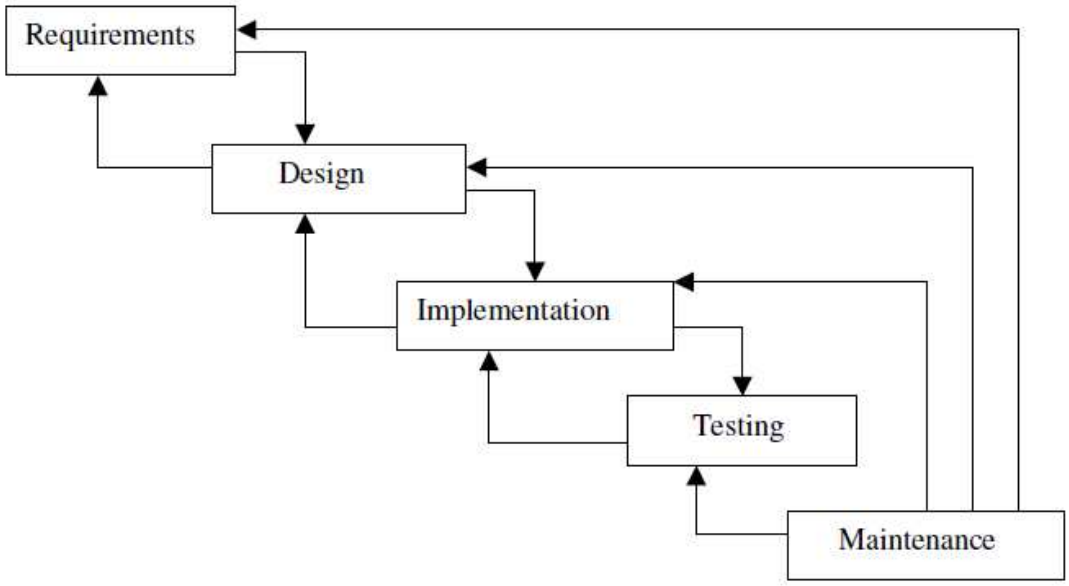
SIXTEEN MARKS

UNIT 1

1. **Explain iterative waterfall and spiral model for software life cycle and various activities in each phase.**

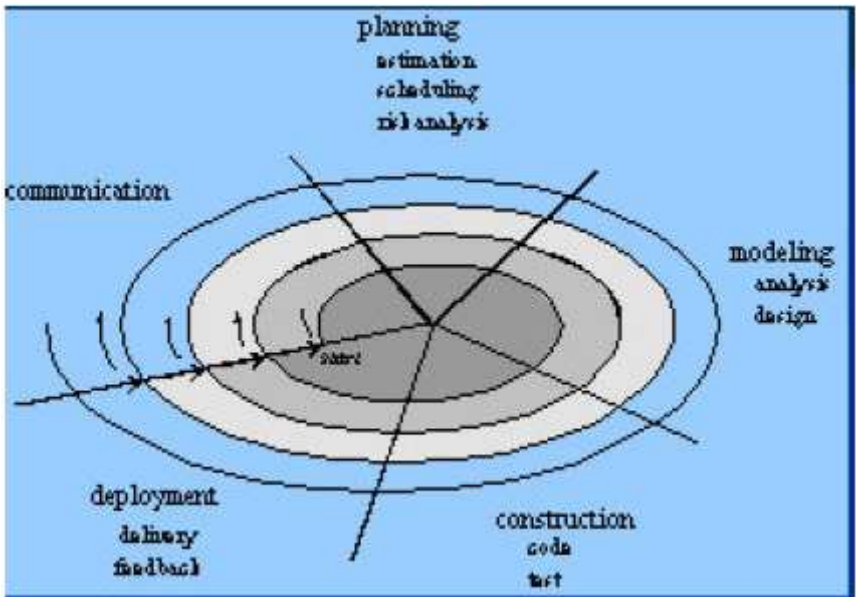
Answer: Iterative waterfall model

The iterative waterfall model is as shown in the following figure.



- Requirement gathering phase in which all requirements are identified.
- The deign phase is responsible for creating architectural view of the software.
- The implementation phase in which the software design is transformed into coding.
- Testing is a kind of phase in which the developed software component is fully tested.
- Maintenance is an activity by which the software product can be maintained.
  - ✓ Requirements
  - ✓ Design
  - ✓ Implementation
  - ✓ Testing
  - ✓ Maintenance

SPIRAL MODEL



The spiral model is divided into number of frame works. These frameworks are denoted by task regions.

- Usually there are six task regions. In spiral model project entry point axis is defined.
- The task regions are:
  - Customer communication
  - Planning
  - Risk analysis.
  - Engineering.
  - Construct and release.
  - Customer evaluation.

Drawbacks

- It is based on customer communication.
- It demands considerable risk assessment**.**

2. Explain about the incremental model.

- Have same phases as the waterfall model.
- Phases are
  - Analysis.
  - Design.
  - Code.
  - Test.
- Incremental model delivers series of releases to customers called as increments.
- The first increment is called as core product. Here only the document processing facilities are available.
- Second increment, more sophisticated document producing and processing facilities are available.
- Next increment spelling and grammar checking facilities are given.

Merits

- This model can be adopted when there is less number of people involved in the project.
- Technical risks can be managed with each increment.
- For a very small time span, at least core product can be delivered to the customer.

RAD Model
- Rapid Application Development Model is the type of incremental model.
- Achieves the high speed development using component based construction.

Phases
- Business modeling
- Data modeling
- Process modeling
- Application generation.
- Testing and turnover**.**

3. Explain in detail about the software process.
- It is defined as the structured set of activities that are required to develop the software system.

Fundamental activities
- Specification
- Design and implementation
- Validation
- Evolution

Common Process Framework
- **Process framework activities**
  - Communication
  - Planning
  - Modeling
  - Construction
  - Deployment.
- **Task Sets**

Defines the actual work to achieve the software objective.
- **Umbrella activities**
  - Software project tracking and control
  - Risk management
  - Software quality assurance
  - Formal technical reviews
  - Software configuration management
  - Work product preparation and production
  - Reusability management.
  - Measurement.

Capability Maturity Model(CMM)

Level 1:Initial – Few processes are defined and individual efforts are taken.

Level 2:Repeatable – To track cost schedule and functionality basic project management processes are established.

Level 3:Defined – The process is standardized, documented and followed.
Level 4:Managed – Both the software process and product are quantitatively understood and controlled using detailed measures.
Level 5:Optimizing – Establish mechanisms to plan and implement change.

4. Explain in detail about the life cycle process.

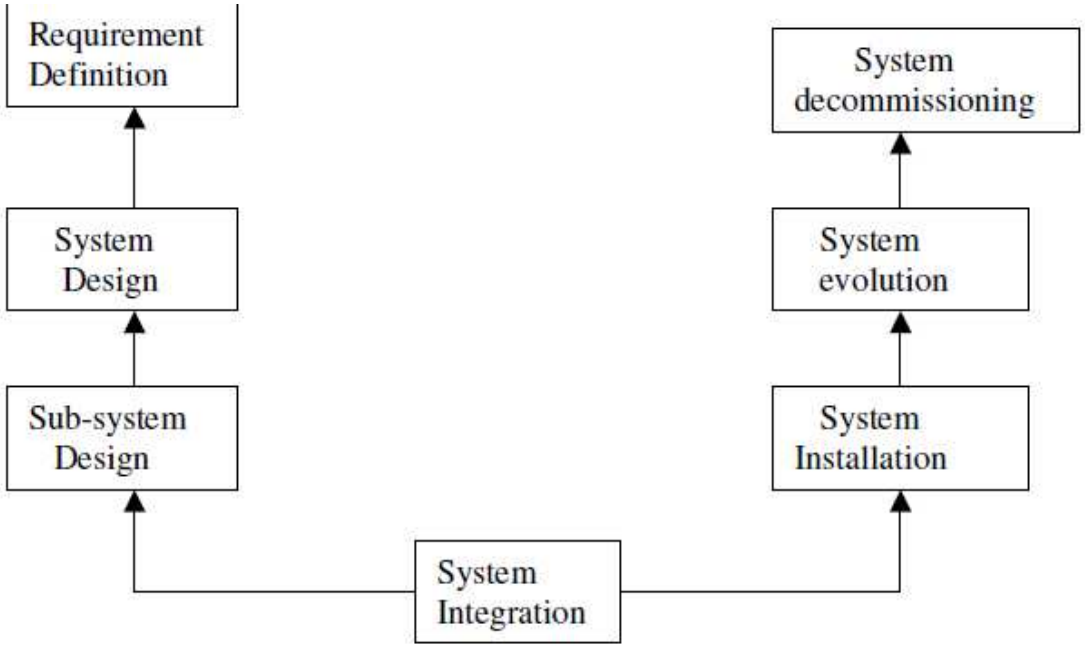


Fig: System engineering process

• System engineering process follows a waterfall model for the parallel development of different parts of the system.

System requirements definition

• Three types of requirements
  - Abstract functional requirements.
  - System properties.
  - Undesirable Characteristics.
• System objectives
• System requirement problem.

The system design process

Process steps

• Partition requirements
• Identify sub-systems.

- Assign requirements to sub-systems.
- Specify sub-system functionality.
- Define sub-system interfaces.

Sub-System development process
- After system design it starts.
- Involve use of COTS (Commercial-Off-The-Shelf).

System Integration
- It is the process of putting hardware, software and people together to make a system.

System Installation

Issues are
- Environmental assumptions may be incorrect.
- There may be human resistance to the introduction of anew system.
- System may have to coexist with alternative systems for some period.
- There may arise some physical installation problems (e.g. cabling problem).
- Operator training has to be identified.

System evolution
- The lifetime of large systems is too long. They must evolve to meet change requirements.
- The evolution may be costly.
- Existing systems that must be maintained are sometimes called as legacy systems.

System Decommissioning
- Taking the system out of service after its useful lifetime is called as System Decommissioning.

UNIT 2:

5. Explain the prototyping approaches in software process.
Two approaches
i. Evolutionary prototyping – In this approach of system development, the initial prototype is prepared and it is then refined through number of stages to final stage.
ii. **Throw-away prototyping –** Using this approach a rough practical implementation of the system is produced. The requirement problems can be identified from this implementation. It is then discarded. System is then developed using some different engineering paradigm.

Evolutionary prototyping
Objective:
- The principal objective of this model is to deliver the working system to the end-user.
- Example-AI systems.

Advantages
- Fast delivery of the working system.
- User is involved while developing the system.
- More useful system can be delivered.
- Specification, design and implementation work is co-ordinated manner.

Problems
- Management problems
- Maintenance problem
- Verification

Incremental Development
- After designing the overall architecture the system is developed and delivered in series of increments.

Throw-away prototyping
Objective:
- The principal objective of this model is to validate or to derive the system requirements.
- It is developed to reduce requirement risks.

Advantages
- Requirement risks are very less.

Problems
- It can be undocumented.
- Changes made during the software development proceed may degrade the system structure.
- Sometimes organizational quality standard may not be strictly applied.

6. **Explain about rapid prototyping techniques.**
Executable specification languages.

- Used to animate the system specification.
- It is expressed in a formal, mathematical language to provide a system prototype.

Very high level languages.

- These are programming languages which include powerful data management facilities.
- They simplify program development.

Application generators and fourth-generation languages.

- These are successful languages because there is a great deal of communality across data processing applications.

7. Explain in detail about data modeling.

- Data modeling makes use of the ERD.
- Consists of 3 interrelated information.

The data object.

- Attributes.
- Relationships.

Cardinality and Modality

- Cardinality is the specification of the number of occurrences of one object that can be related to the number of occurrences of another object.
- One-to-one cardinality.
- One-to-many cardinality.
- Many-to-Many cardinality.
- Modality of a relation is 0 if there is no explicit relationship or relation is optional.
- Modality is 1 if an occurrence of relationship is mandatory.

Entity/Relationship Diagrams

- Components are
  - Data Objects.
  - Attributes.
  - Relationships.
  - Various type indicators.
  -

8. Explain in detail about Functional Modeling.

- This model describes the computations that take place within a system.
- This model is useful when the transformation from the inputs to outputs is complex.
- The functional model of a system can be represented by a data Flow Diagram(DFD).

Data Flow Diagrams/Data Flow Graph/Bubble chart

- A DFD is a graphical representation that depicts the information flow and the transforms that are applied as the data move from input to output.
- Level 0 DFD also called as fundamental system model or context model represents the entire software as a single bubble with input and output data indicated by incoming and outgoing arrows.
- Level 1 DFD contains 5 or 6 bubbles. Each bubbles can be refined at Layers to depict more details.

Extensions to Real Time Systems

- Ward and Meller extensions
- Hatley and Pirbhai extension.

9. Explain in detail about Structural Modeling.

- Structural model includes a detail refinement of ERD,data flow model and control flow model.
- Creating an ERD.
- Example: Safe Home Security System.
- Developing relationships and cardinality/Modality.
- Creating a data flow model using the guidelines.
- Creating a control flow model which describes the structural connection of Processes Control flows

Control stores.

- State automation
- Process activation table.

UNIT 3:

10. Explain in detail the design concepts.

Abstraction

- Functional abstraction
- Data abstraction
- Control abstraction

Information hiding

- Each module in the system hides the internal details of its processing activities and modules communicate only through over defined interfaces.

Structure

- It permits the decomposition of a large system into smaller, more manageable units with well defined relationships to the other units in a system.
- Network is the most general form of structure.

Hierarchical Structures/Structure Charts

- It depicts the structure of subroutines in a system, the data passed between routines, can be indicated on the arcs connecting routines.

Modularity

- Modular system consists of well-defined, manageable units with well defined interfaces among units.

Concurrency

- Independent processes that can be activated simultaneously if multiple processors are available.

Coupling and Cohesion

- **Data coupling –** The data coupling is possible by parameter passing or data interaction.
- **Control coupling –** The modules share related control data in control coupling.
- **Common coupling –** The common data or a global data is shared among modules.
- **Content coupling** – Content coupling occurs when one module makes use of data or control information maintained in another module.

11. Explain the design principles.

- The design process should not suffer from tunnel vision.
- The design should be traceable to the analysis model.
- Design should not reinvent the wheel.
- The design should minimize the intellectual distance between the software and problem as it exists in the real world.
- The design should be structured to degrade gently, even when aberrant data, events or operating conditions are encountered.
- Design is not coding, coding is not design.
- The design should be assessed for quality as it is being created, not after the fact.
- The design should be reviewed to minimize conceptual (semantic) errors.

12. Explain the design steps of the transform mapping.

- Review the fundamental model.
- Review and refine the DFD for the software.
- Determine whether the DFD has the transform or transaction mapping.
- Isolate the transform center by specifying incoming and outgoing flow boundaries.
- Perform first-level factoring.
- Perform second-level factoring.
- Refine the first iteration architecture using design heuristics for improved software quality.

13. Explain the design steps in transaction mapping.

- Review the fundamental model.
- Review and refine the DFD for the software.
- Determine whether the DFD has the transform or transaction mapping.
- Identify transaction center and the flow characteristics along each of the action paths.
- Factor and refine the transaction structure and the structure of each action path.
- Refine the first iteration architecture using design heuristics for improved software quality.

14. Explain in detail about the real time systems.

- Hard and soft real time systems.
- Real time and high performance.
- Real-Time control.
- Real time software design

Periodic Stimuli – Occur at predictable time intervals.
Aperiodic Stimuli – Occur regularly

UNIT 4:

15. Explain the types of software testing.

- Unit testing
- System testing
- Integration testing
- User-acceptance testing
- End-to-End testing
- Regression testing
- Exception testing
- Destructive testing

16. Explain in detail about Black box testing.

- Black box or behavioral testing focuses on the functional requirements of the software.
- It is applied during the last stage of testing.
- Syntax driven testing is suitable for the specification which are described by a certain grammar.
- Decision table based testing is implemented when the original software requirement have been formulated in the format of " if-then" statements.
- Liquid level control is the study of a simple control problem which is designed to check the liquid level. It has 2 sensors.
- Cause effect graphs in functional testing.

17. Explain about the software testing strategies.

- A strategic approach to software testing.
- Verification and Validation. Verification refers to the set of activities that ensure that software correctly implements a specific function. Validation refers to a different set of activities that ensure that the software that has been built is traceable to the customer requirements.

According to Boehm, Verification:" Are we building the product right?" Validation:" Are we building the right product?"

- Organization for software testing
- A software testing strategy.
- Criteria for completion of testing.

18. Explain in detail about Integration testing.

- It is a systematic technique for constructing the program structure.
- **Incremental integration –** The program is constructed and tested in small increments.

Top-down integration

- It is an incremental approach.
- Modules are integrated by moving downward through the control hierarchy beginning with the main control module(main program).
- Subordinate modules are incorporated by depth-first or breadth-first manner.

Bottom-up integration

- This testing begins construction and testing with the components at the lowest levels in the program structure.

Regression testing

- It is the re-execution of some subset of tests that have already been conducted to ensure the changes that have not been propagated unintended side effects.

Smoke testing

- It minimizes the integration risk.
- Error diagnosis and correction are simplified.

19. Explain in detail about system testing.

- System testing
- Stress testing
- Security testing.
- Performance testing

UNIT 5:

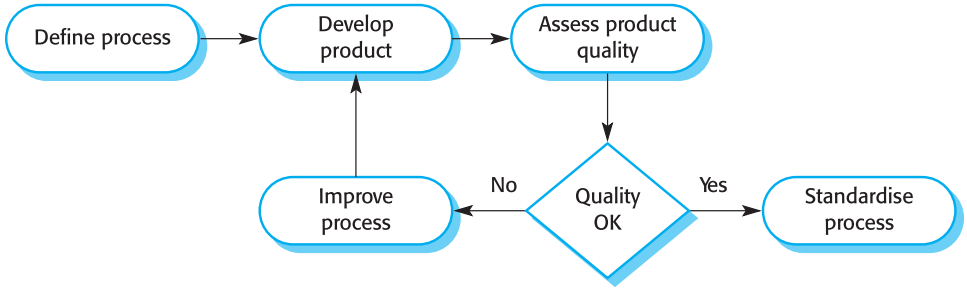
19.Explain Process and product quality(8marks)

●The quality of a developed product is influenced by the quality of the production process.

●This is important in software development as some product quality attributes are hard to assess.

●However, there is a very complex and poorly understood relationship between software processes and product quality.

Process-based quality



●There is a straightforward link between process and product in manufactured goods.

●More complex for software because:

•The application of individual skills and experience is particularly imporant in software development;

•External factors such as the novelty of an application or the need for an accelerated development schedule may impair product quality.

●Care must be taken not to impose inappropriate process standards - these could reduce rather than improve the product quality.

Practical process quality

●Define process standards such as how reviews should be conducted, configuration management, etc.

●Monitor the development process to ensure that standards are being followed.

●Report on the process to project management and software procurer.

●Don't use inappropriate practices simply because standards have been established.

Quality assurance and standards

●Standards are the key to effective quality management.

●They may be international, national, organizational or project standards.

●Product standards define characteristics that all components should exhibit e.g. a common programming style.

●Process standards define how the software process should be enacted.

Importance of standards

●Encapsulation of best practice- avoids repetition of past mistakes.

- They are a framework for quality assurance processes - they involve checking compliance to standards.
- They provide continuity - new staff can understand the organisation by understanding the standards that are used.

Product and process standards

Problems with standards

- They may not be seen as relevant and up-to-date by software engineers.
- They often involve too much bureaucratic form filling.
- If they are unsupported by software tools, tedious manual work is often involved to maintain the documentation associated with the standards.

Standards development

- Involve practitioners in development. Engineers should understand the rationale underlying a standard.
- Review standards and their usage regularly. Standards can quickly become outdated and this reduces their credibility amongst practitioners.
- Detailed standards should have associated tool support. Excessive clerical work is the most significant complaint against standards.

20. Explain ISO 9000 and Documentation Standard

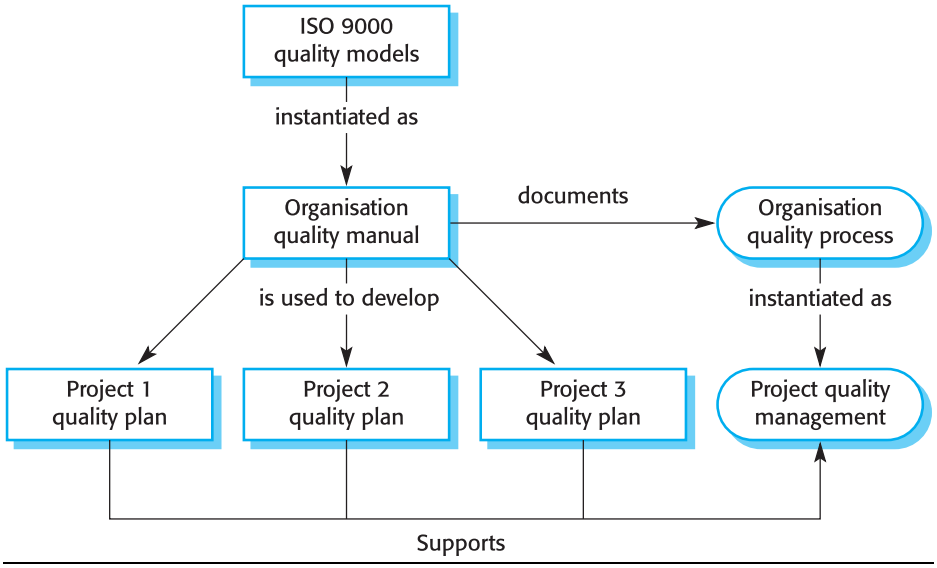
ISO 9000

- An international set of standards for quality management.
- Applicable to a range of organisations from manufacturing to service industries.
- ISO 9001 applicable to organisations which design, develop and maintain products.
- ISO 9001 is a generic model of the quality process that must be instantiated for each organisation using the standard.

ISO 9000 certification

- Quality standards and procedures should be documented in an organisational quality manual.
- An external body may certify that an organisation's quality manual conforms to ISO 9000 standards.
- Some customers require suppliers to be ISO 9000 certified although the need for flexibility here is increasingly recognised.

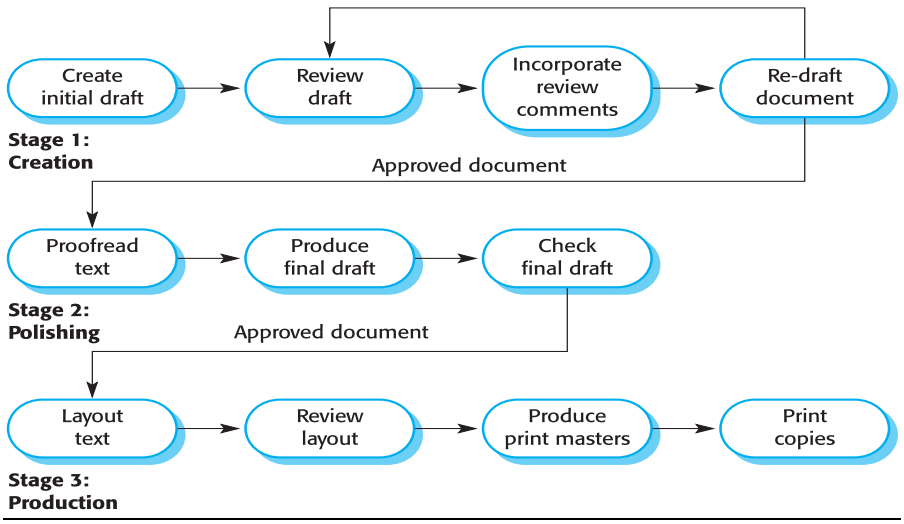
ISO 9000 and quality management



Documentation standards

- Particularly important - documents are the tangible manifestation of the software.
- Documentation process standards
  - Concerned with how documents should be developed, validated and maintained.
- Document standards
  - Concerned with document contents, structure, and appearance.
- Document interchange standards
  - Concerned with the compatibility of electronic documents.

Documentation process



Document standards

- Document identification standards
  - How documents are uniquely identified.

●Document structure standards
•Standard structure for project documents.
●Document presentation standards
•Define fonts and styles, use of logos, etc.
●Document update standards
•Define how changes from previous versions are reflected in a document.

Document interchange standards

●Interchange standards allow electronic documents to be exchanged, mailed, etc.
●Documents are produced using different systems and on different computers. Even when standard tools are used, standards are needed to define conventions for their use e.g. use of style sheets and macros.
●Need for archiving. The lifetime of word processing systems may be much less than the lifetime of the software being documented. An archiving standard may be defined to ensure that the document can be accessed in future.

21. Explain the quality control.

Quality control

●This involves checking the software development process to ensure that procedures and standards are being followed.
●There are two approaches to quality control
•Quality reviews;
•Automated software assessment and software measurement.

Quality reviews

●This is the principal method of validating the quality of a process or of a product.
●A group examines part or all of a process or system and its documentation to find potential problems.
●There are different types of review with different objectives
•Inspections for defect removal (product);
•Reviews for progress assessment (product and process);
•Quality reviews (product and standards).

Types of review

Review type	**Principal purpose**
Design or program inspections	To detect detailed errors in the requirements, design or code. A checklist of possible errors should drive the review.
Progress reviews	To provide information for management about the overall progress of the project. This is both a process and a product review and is concerned with costs, plans and schedules.

Quality reviews	To carry out a technical analysis of product components or documentation to find mismatches between the specification and the component design, code or documentation and to ensure that defined quality standards have been followed.

Quality reviews

- A group of people carefully examine part or all of a software system and its associated documentation.
- Code, designs, specifications, test plans, standards, etc. can all be reviewed.
- Software or documents may be 'signed off' at a review which signifies that progress to the next development stage has been approved by management.

Review functions

- Quality function - they are part of the general quality management process.
- Project management function - they provide information for project managers.
- Training and communication function - product knowledge is passed between development team members.

Quality reviews

- The objective is the discovery of system defects and inconsistencies.
- Any documents produced in the process may be reviewed.
- Review teams should be relatively small and reviews should be fairly short.
- Records should always be maintained of quality reviews.

Review results

- Comments made during the review should be classified
  - No action. No change to the software or documentation is required;
  - Refer for repair. Designer or programmer should correct an identified fault;
  - Reconsider overall design. The problem identified in the review impacts other parts of the design. Some overall judgement must be made about the most cost-effective way of solving the problem;
- Requirements and specification errors may have to be referred to the client.

22.Explain Software measurement and metrics

Software measurement and metrics

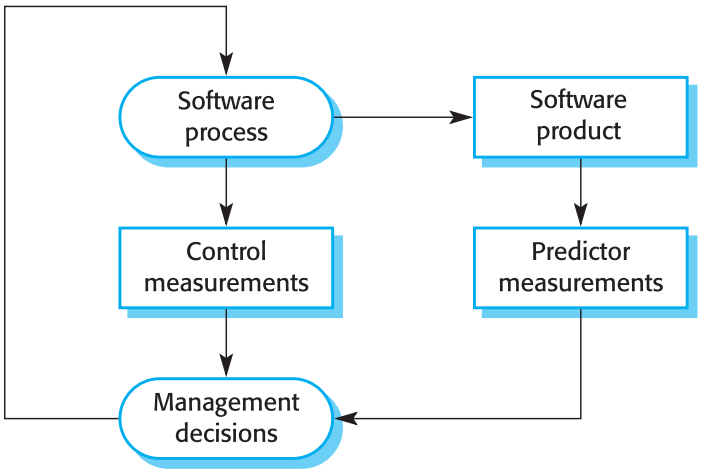
- Software measurement is concerned with deriving a numeric value for an attribute of a software product or process.
- This allows for objective comparisons between techniques and processes.
- Although some companies have introduced measurement programmes, most organisations still don't make systematic use of software measurement.
- There are few established standards in this area.

Software metric

- Any type of measurement which relates to a software system, process or related documentation
  - Lines of code in a program, the Fog index, number of person-days required to develop a component.
- Allow the software and the software process to be quantified.
- May be used to predict product attributes or to control the software process.

•Product metrics can be used for general predictions or to identify anomalous components.

Predictor and control metrics



Metrics assumptions

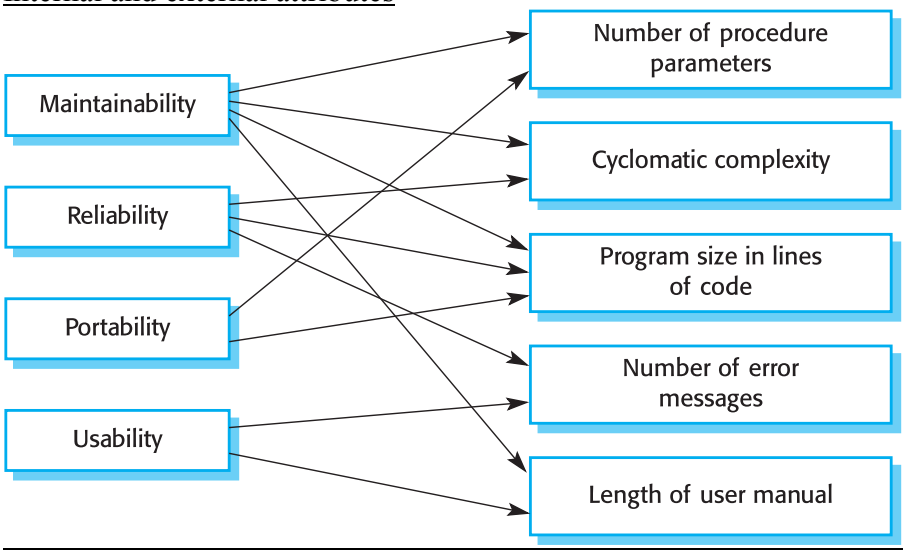
•A software property can be measured.

•The relationship exists between what we can measure and what we want to know. We can only measure internal attributes but are often more interested in external software attributes.

•This relationship has been formalised and validated.

•It may be difficult to relate what can be measured to desirable external quality attributes.

Internal and external attributes



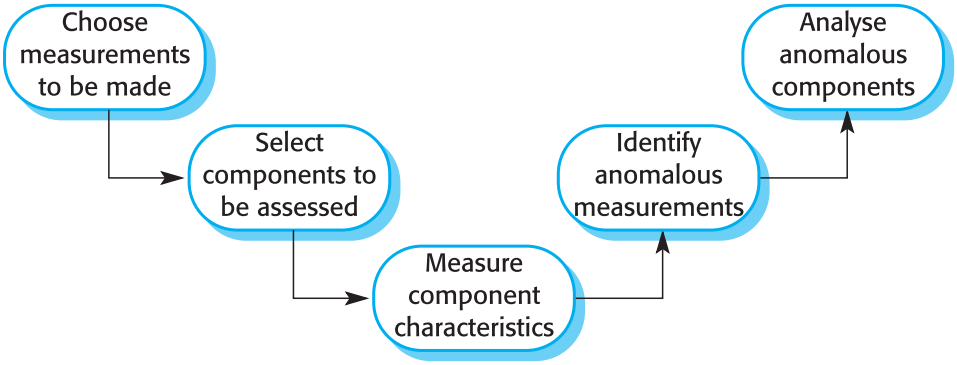
The measurement process

•A software measurement process may be part of a quality control process.

•Data collected during this process should be maintained as an organisational resource.

•Once a measurement database has been established, comparisons across projects become possible.

Product measurement process



Data collection

- A metrics programme should be based on a set of product and process data.
- Data should be collected immediately (not in retrospect) and, if possible, automatically.
- Three types of automatic data collection
  - Static product analysis;
  - Dynamic product analysis;
  - Process data collation.

Data accuracy

- Don't collect unnecessary data
  - The questions to be answered should be decided in advance and the required data identified.
- Tell people why the data is being collected.
  - It should not be part of personnel evaluation.
- Don't rely on memory
  - Collect data when it is generated not after a project has finished.

Product metrics

- A quality metric should be a predictor of product quality.
- Classes of product metric
  - Dynamic metrics which are collected by measurements made of a program in execution;
  - Static metrics which are collected by measurements made of the system representations;
  - Dynamic metrics help assess efficiency and reliability; static metrics help assess complexity, understandability and maintainability.

Dynamic and static metrics

- Dynamic metrics are closely related to software quality attributes
  - It is relatively easy to measure the response time of a system (performance attribute) or the number of failures (reliability attribute).
- Static metrics have an indirect relationship with quality attributes
  - You need to try and derive a relationship between these metrics and properties such as complexity, understandability and maintainability.

Software product metrics

Software metric	Description

Fan in/Fan-out	Fan-in is a measure of the number of functions or methods that call some other function or method (say X). Fan-out is the number of functions that are called by function X. A high value for fan-in means that X is tightly coupled to the rest of the design and changes to X will have extensive knock-on effects. A high value for fan-out suggests that the overall complexity of X may be high because of the complexity of the control logic needed to coordinate the called components.
Length of code	This is a measure of the size of a program. Generally, the larger the size of the code of a component, the more complex and error-prone that component is likely to be. Length of code has been shown to be one of the most reliable metrics for predicting error-proneness in components.
Cyclomatic complexity	This is a measure of the control complexity of a program. This control complexity may be related to program understandability. I discuss how to compute cyclomatic complexity in Chapter 22.
Length of identifiers	This is a measure of the average length of distinct identifiers in a program. The longer the identifiers, the more likely they are to be meaningful and hence the more understandable the program.
Depth of conditional nesting	This is a measure of the depth of nesting of if-statements in a program. Deeply nested if statements are hard to understand and are potentially error-prone.
Fog index	This is a measure of the average length of words and sentences in documents. The higher the value for the Fog index, the more difficult the document is to understand.

Object-oriented metrics

Object-oriented metric	Description
Depth of inheritance tree	This represents the number of discrete levels in the inheritance tree where sub-classes inherit attributes and operations (methods) from super-classes. The deeper the inheritance tree, the more complex the design. Many different object classes may have to be understood to understand the object classes at the leaves of the tree.
Method fan-in/fan-out	This is directly related to fan-in and fan-out as described above and means essentially the same thing. However, it may be appropriate to make a distinction between calls from other methods within the object and calls from external methods.
Weighted methods per class	This is the number of methods that are included in a class weighted by the complexity of each method. Therefore, a simple method may have a complexity of 1 and a large and complex method a much higher value. The larger the value for this metric, the more complex the object class. Complex objects are more

	likely to be more difficult to understand. They may not be logically cohesive so cannot be reused effectively as super-classes in an inheritance tree.
Number of overriding operations	This is the number of operations in a super-class that are over-ridden in a sub-class. A high value for this metric indicates that the super-class used may not be an appropriate parent for the sub-class.

Measurement analysis

- It is not always obvious what data means
- Analysing collected data is very difficult.
- Professional statisticians should be consulted if available.
- Data analysis must take local circumstances into account.

Measurement surprises

- Reducing the number of faults in a program leads to an increased number of help desk calls
- The program is now thought of as more reliable and so has a wider more diverse market. The percentage of users who call the help desk may have decreased but the total may increase;
- A more reliable system is used in a different way from a system where users work around the faults. This leads to more help desk calls.

23.Explain process improvement stages.

Process improvement stages

- Process measurement
- Attributes of the current process are measured. These are a baseline for assessing improvements.
- Process analysis
- The current process is assessed and bottlenecks and weaknesses are identified.
- Process change
- Changes to the process that have been identified during the analysis are introduced.

Process measurement

- Wherever possible, quantitative process data should be collected
- However, where organisations do not have clearly defined process standards this is very difficult as you don't know what to measure. A process may have to be defined before any measurement is possible.
- Process measurements should be used to assess process improvements
- But this does not mean that measurements should drive the improvements. The improvement driver should be the organizational objectives.

Classes of process measurement

- Time taken for process activities to be completed
- E.g. Calendar time or effort to complete an activity or process.
- Resources required for processes or activities
- E.g. Total effort in person-days.
- Number of occurrences of a particular event
- E.g. Number of defects discovered.

Goal-Question-Metric Paradigm

- Goals
  - What is the organisation trying to achieve? The objective of process improvement is to satisfy these goals.
- Questions
  - Questions about areas of uncertainty related to the goals. You need process knowledge to derive these.
- Metrics
  - Measurements to be collected to answer the questions.

Process analysis and modelling

- Process analysis
  - The study of existing processes to understand the relationships between parts of the process and to compare them with other processes.
- Process modelling
  - The documentation of a process which records the tasks, the roles and the entities used;
  - Process models may be presented from different perspectives.

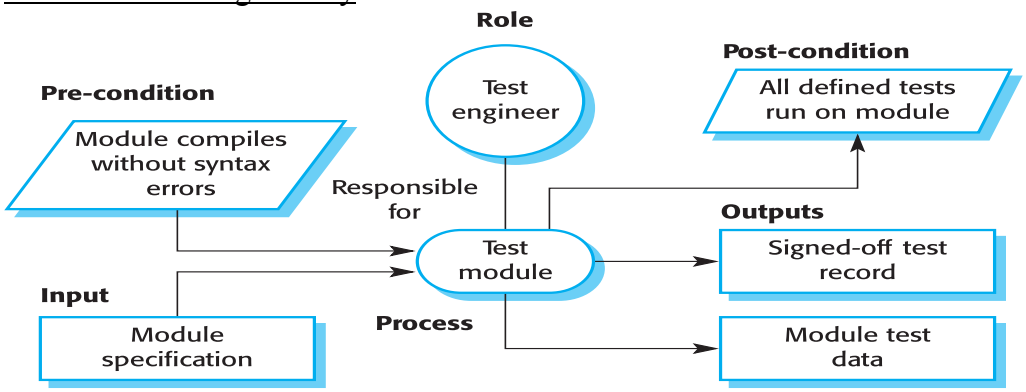
Process analysis and modelling

- Study an existing process to understand its activities.
- Produce an abstract model of the process. You should normally represent this graphically. Several different views (e.g. activities, deliverables, etc.) may be required.
- Analyse the model to discover process problems. This involves discussing process activities with stakeholders and discovering problems and possible process changes.

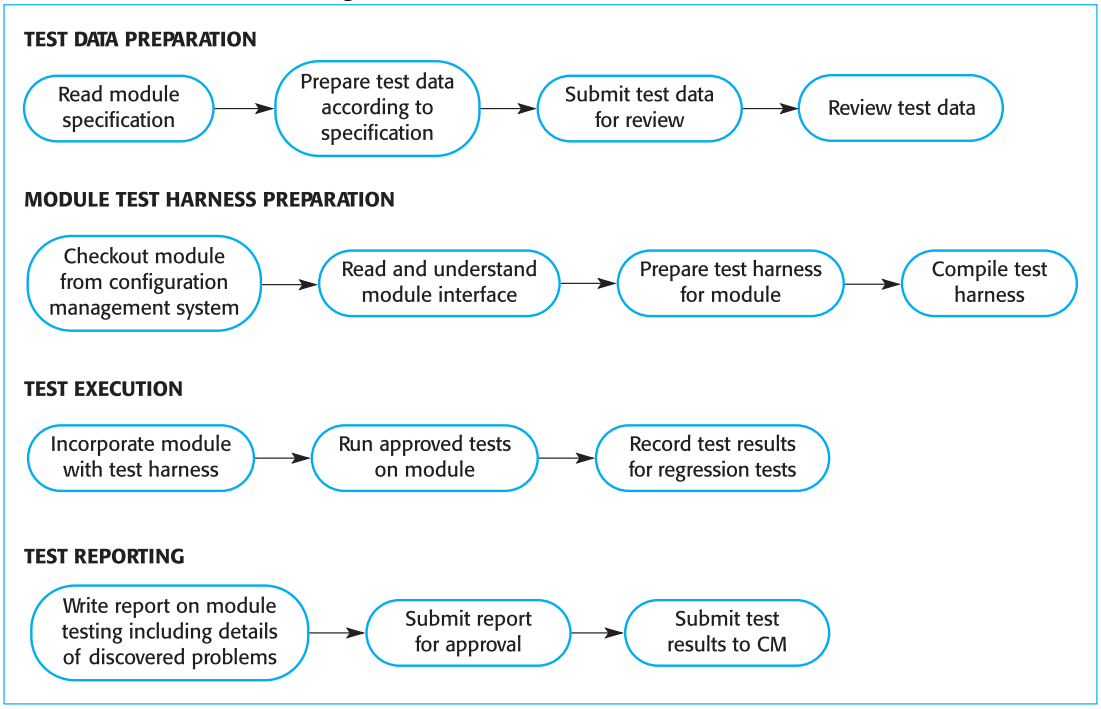
Process analysis techniques

- Published process models and process standards
  - It is always best to start process analysis with an existing model. People then may extend and change this.
- Questionnaires and interviews
  - Must be carefully designed. Participants may tell you what they think you want to hear.
- Ethnographic analysis
  - Involves assimilating process knowledge by observation. Best for in-depth analysis of process fragments rather than for whole-process understanding.

The module testing activity



Activities in module testing



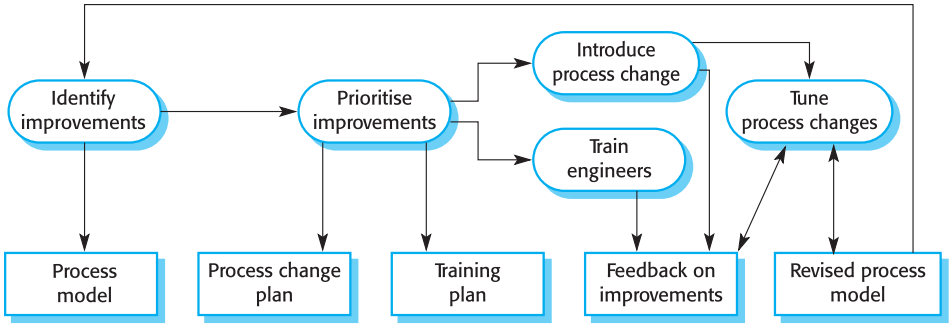
Process exceptions

- Software processes are complex and process models cannot effectively represent how to handle exceptions:
  - Several key people becoming ill just before a critical review;
  - A breach of security that means all external communications are out of action for several days;
  - Organisational reorganisation;
  - A need to respond to an unanticipated request for new proposals.
- Under these circumstances, the model is suspended and managers use their initiative to deal with the exception.

Process change

- Involves making modifications to existing processes.
- This may involve:
  - Introducing new practices, methods or processes;
  - Changing the ordering of process activities;
  - Introducing or removing deliverables;
  - Introducing new roles or responsibilities.
- Change should be driven by measurable goals.

The process change process



Process change stages

- Improvement identification.
- Improvement prioritisation.
- Process change introduction.
- Process change training.
- Change tuning.

24.Explain CMMI.

The CMMI framework

- The CMMI framework is the current stage of work on process assessment and improvement that started at the Software Engineering Institute in the 1980s.
- The SEI's mission is to promote software technology transfer particularly to US defence contractors.
- It has had a profound influence on process improvement
  - Capability Maturity Model introduced in the early 1990s.
  - Revised maturity framework (CMMI) introduced in 2001.

The CMMI model

- An integrated capability model that includes software and systems engineering capability assessment.
- The model has two instantiations
  - Staged where the model is expressed in terms of capability levels;
  - Continuous where a capability rating is computed.

CMMI model components

- Process areas

  24 process areas that are relevant to process capability and improvement are identified. These are organised into 4 groups.
- Goals

  Goals are descriptions of desirable organisational states. Each process area has associated goals.
- Practices

  Practices are ways of achieving a goal - however, they are advisory and other approaches to achieve the goal may be used.

CMMI process areas 1

Process management	Organisational process definition Organisational process focus Organisational training Organisational process performance Organisational innovation and deployment
Project management	Project planning Project monitoring and control Supplier agreement management Integrated project management Risk management Integrated teaming Quantitative project management

CMMI process areas 2

Engineering	Requirements management Requirements development Technical solution Product integration Verification Validation
Support	Configuration management Process and product quality management Measurement and analysis Decision analysis and resolution Organisational environment for integration Causal analysis and resolution

CMMI goals

Goal	**Process area**
Corrective actions are managed to closure when the project's performance or results deviate significantly from the plan.	Specific goal in Project Monitoring and Control
Actual performance and progress of the project is monitored against the project plan.	Specific goal in project monitoring and control
The requirements are analyzed and validated and a definition of the required functionality is developed.	Specific goal in requirements development.
Root causes of defects and other problems are systematically determined.	Specific goal in causal analysis and resolution.
The process is institutionalized as a	Generic goal

defined process.

CMMI practices

Practice	Associated goal
Analyse derived requirements to ensure that they are necessary and sufficient	The requirements are analysed and validated and a definition of the required functionality is developed.
Validate requirements to ensure that the resulting product will perform as intended in the user's environment using multiple techniques as appropriate.	
Select the defects and other problems for analysis.	Root causes of defects and other problems are systematically determined.
Perform causal analysis of selected defects and other problems and propose actions to address them.	
Establish and maintain an organisational policy for planning and performing the requirements development process.	The process is institutionalised as a defined process.
Assign responsibility and authority for performing the process, developing the work products and providing the services of the requirements development process.	

CMMI assessment

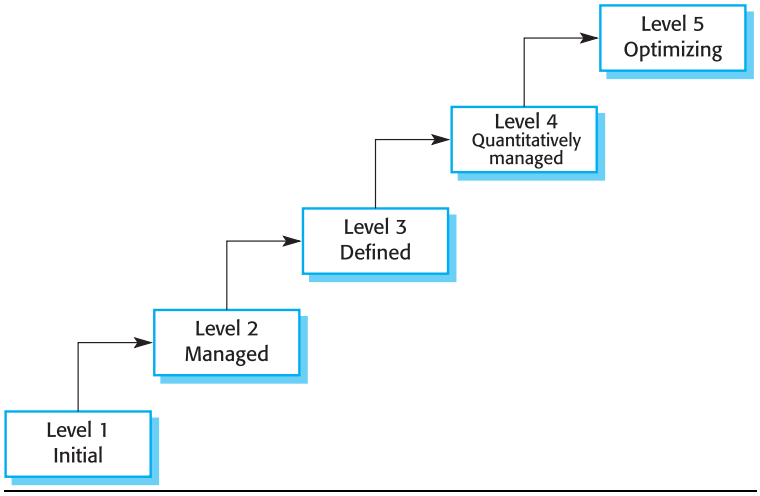
- Examines the processes used in an organisation and assesses their maturity in each process area.
- Based on a 6-point scale:
  - Not performed;
  - Performed;
  - Managed;
  - Defined;
  - Quantitatively managed;
  - Optimizing.

The staged CMMI model

- Comparable with the software CMM.
- Each maturity level has process areas and goals. For example, the process area associated with the managed level include:
  - Requirements management;
  - Project planning;
  - Project monitoring and control;
  - Supplier agreement management;
  - Measurement and analysis;

•Process and product quality assurance.

The staged CMMI model



Institutional practices

•Institutions operating at the managed level should have institutionalised practices that are geared to standardisation.

•Establish and maintain policy for performing the project management process;

•Provide adequate resources for performing the project management process;

•Monitor and control the project planning process;

•Review the activities, status and results of the project planning process.

The continuous CMMI model

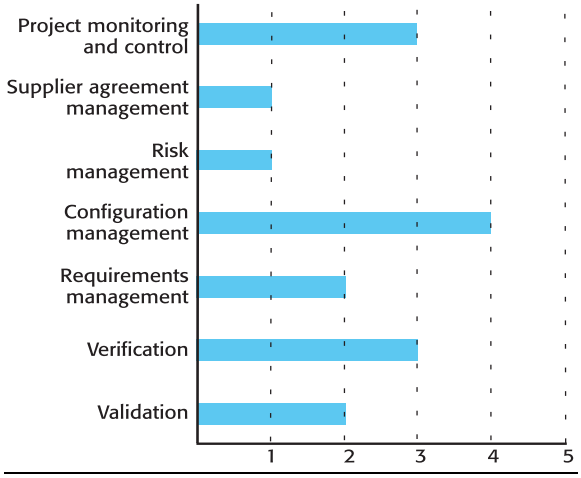
•This is a finer-grain model that considers individual or groups of practices and assesses their use.

•The maturity assessment is not a single value but is a set of values showing the organisations maturity in each area.

•The CMMI rates each process area from levels 1 to 5.

•The advantage of a continuous approach is that organisations can pick and choose process areas to improve according to their local needs.

A process capability profile



25. Explain in detail about SCM.

• Software Configuration Management is an umbrella activity that is applied throughout the software process.

SCM Activities

• Identify change.
• Control change.
• Ensure the change is properly implemented.
• Report change to others.

Need for SCM

• When you build computer software change happens, you need to control it effectively.

SCI

• Software Configuration Item is information that is carried as part of the software engineering process.

MODEL QUESTION PAPER
SOFTWARE ENGINEERING

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A - (10 x 2 = 20 marks)

1. Distinguish between Verification and Validation?
2. Define a system and computer-based system?
3. What is cardinality and modality?
4. Create a data dictionary that provides with a precise definition of telephone number, it should indicate, where and how this data item is used and any supplementary information that is relevant to it?
5. What is an architectural style?
6. Describe principles of management?
7. Define Cyclomatic complexity?
8. Difference between White box and Black box testing?
9. List out any two functions of a CASE tool?
10. What is reverse engineering?

PART B - (5 x 16 = 80 marks)

11. (a) Explain the spiral model? 'What are the task regions in the spiral model?

Or

(b) Explain the system engineering hierarchy? What does a System Engineering model accomplish?

12. (a) Explain software prototyping? What are the various prototyping methods and tools?

OR

(b) Explain with example diagram the functional and behavioral modeling.

13. (a) Describe Transform and Transactional mapping by applying design steps to an example system.

OR

(b) Explain Architecture styles.(8)

(ii) Explain the two qualitative criteria - Coupling and Cohesion. (8)

14. (a) (i) Explain cyclomatic complexity. (8)

(ii) Explain integration testing. (8)

OR

(b) Explain the various types of black-box testing methods.

15. Explain in detail about SCM.

OR

Explain CMMI.

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PAR'I' A — (10 × 2 = 20 marks)

1. Write any two software engineering challenges.

2. Identify in which phase of the software life cycle the following documents are delivered.
   (a) Architectural design
   (b) Test plan
   (c) Cost estimate
   (d) Source code document.

3. Define the terms product and process in software engineering.

4. List out the elements of analysis model.

5. What are the types of coupling?

6. Name the three levels of abstraction, which are in practice for the design.

7. Assume a program for computing the roots of a quadratic equation. List out the test cases using equivalence partitioning method.

8. Write the steps involved in testing real time systems.

9. What is CMMI framework?

10. What is Dynamic and static metrics ?

PART B — (5 × 16 = 80 marks)

11. (a) Explain the linear software life cycle model with suitable illustration. Bring out the demerits of this model. (16)

Or

(b) (i) How do you differentiate software engineering from system engineering? (6)

(ii) For each of the types of process models, identify the types of project suitable to implement. (6)

(iii) Distinguish between verification and validation process. (4)

12. (a) (i) With a suitable example explain about the application of use cases in deriving the scenarios. (8)

(ii) Explain the various prototyping methods and tools used for requirement analysis. (8)

Or

(b) Discuss in detail about the elements in data modeling. (16)

13. (a) What are different types of architectural styles exist for software and explain any one software architecture in detail. (16)

Or

(b) (i) Describe activities of SCM in detail. (8)

(ii) Explain the user interface design activities. (8)

14. (a) (i) Why is testing important? (6)

(ii) Narrate the path testing procedure in detail with a sample code. (10)

Or

(b) (i) Distinguish between black box and white box testing. (6)

(ii) Explain the different integration testing approaches. (10)

15. Explain ISO 9000 and Documentation Standard

OR

Explain the quality control